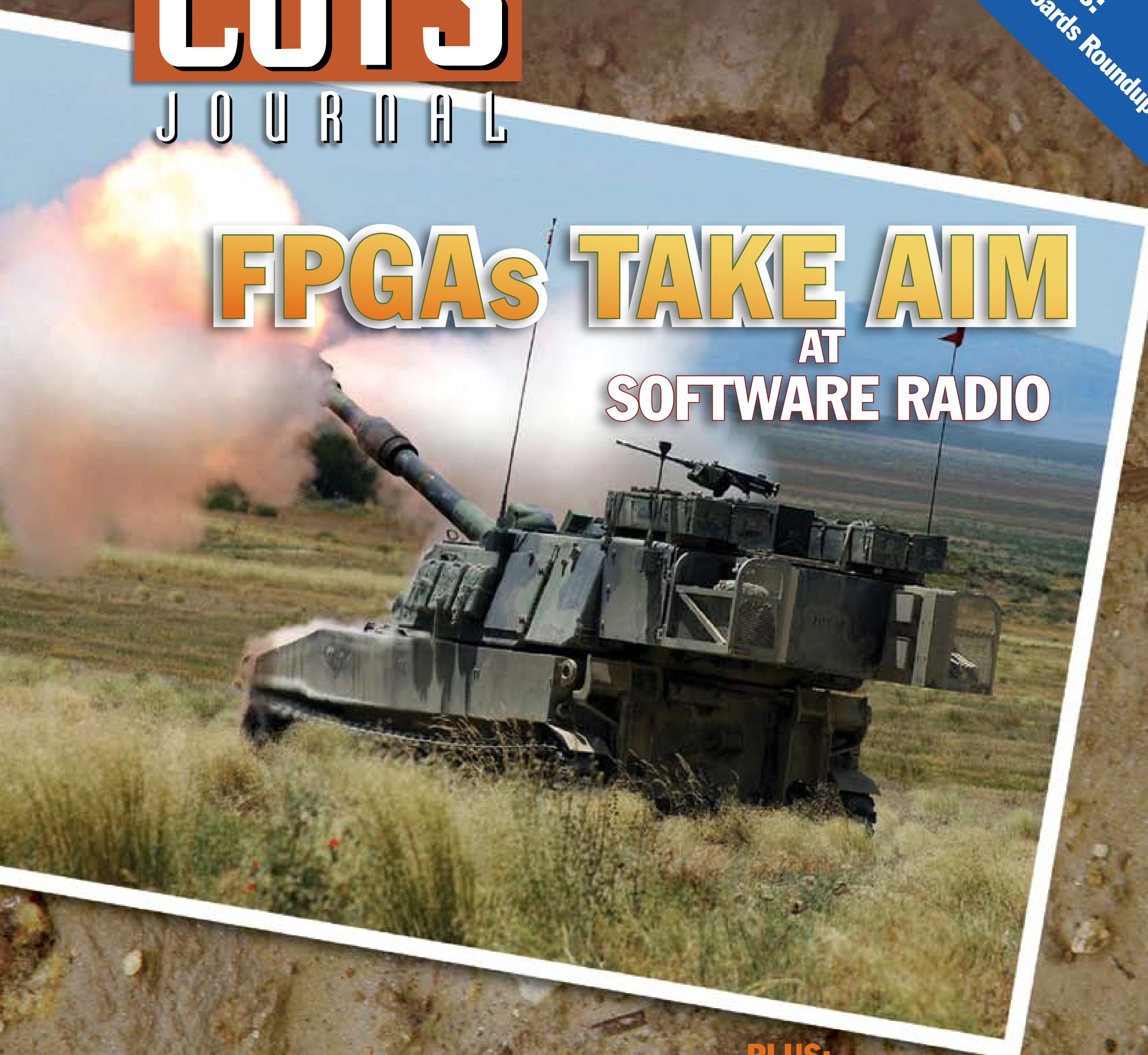
COTS® JOURNAL

Tech Focus: PC/104 and EPIC Boards Roundup



FPGAs TAKE AIM AT SOFTWARE RADIO

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COM 4	RS-232	NA	RS-232
COM 5	RS-232/422/285	NA	NA
COM6	RS-422/485/TTL	NA	NA
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EIDE	2	2	1
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CRT	1600 X 1200	1280 X 1024	1280 X 1024
Flat panel	LVDS	yes	yes
Digital I/O	24-bit prog.	48-bit prog.	24-bit prog.
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Features

October 2006 Volume 8 Number 10

Main Feature

Tech Recon

System Development

Technology Focus

COTS (kots), *n.* **1.** Commercial off-the-shelf. Terminology popularized in 1994 within U.S. DoD by SECDEF Wm. Perry's "Perry Memo" that changed military industry purchasing and design guidelines, making Mil-Specs acceptable only by waiver. COTS is generally defined for technology, goods and services as: a) using commercial business practices and specifications, b) not developed under government funding, c) offered for sale to the general market, d) still must meet the program ORD. **2.** Commercial business practices include the accepted practice of customer-paid minor modification to standard COTS products to meet the customer's unique requirements.

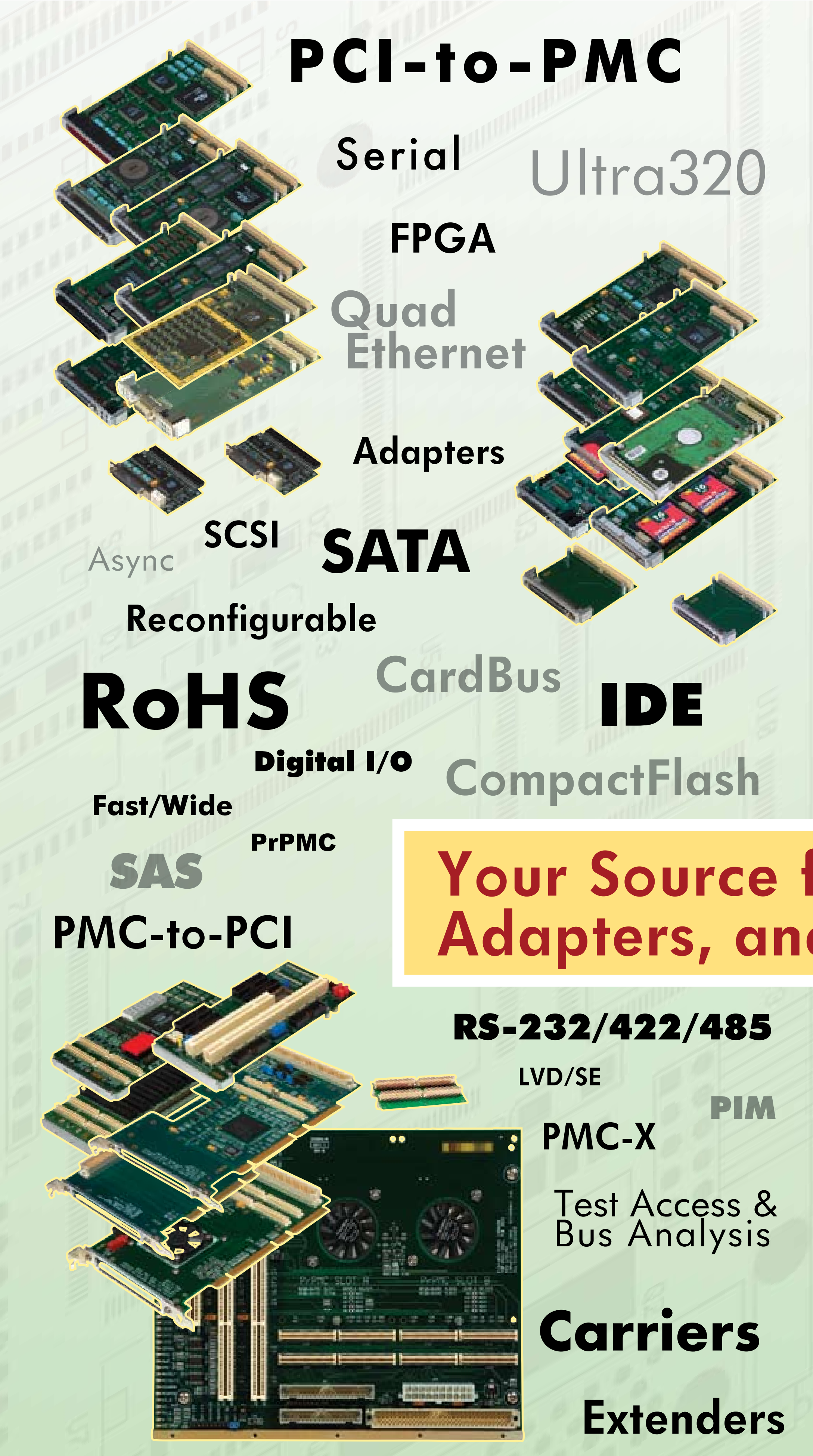
——**Ant.** When applied to the procurement of electronics for the U.S. Military, COTS is a procurement philosophy and does not imply commercial, office environment or any other durability grade. *E.g., rad-hard components designed and offered for sale to the general market are COTS if they were developed by the company and not under government funding.*

Departments

Coming in November...
...See Page 77

Cover Story .... Page 14
An M109A6 Paladin Self Propelled Howitzer is shown here showing off its capabilities during an 04 Patriot exercise at the Dugway Proving Grounds, Dugway, Utah. Paladin features include an Automatic Fire Control System with onboard ballistic computation and automatic weapon pointing, an integrated inertial navigation system with embedded GPS processing, NBC protection with climate control, hydraulics system segregation, and secure voice and digital communications.

Courtesy: DoD Photo by TSGT Michael Rice, USAF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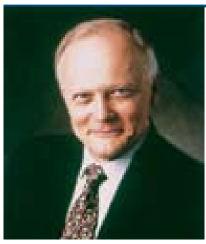
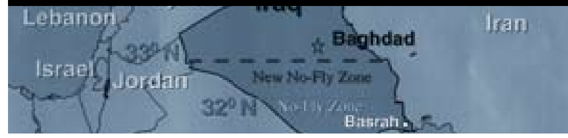




The Military, Juggling and Buses

Turmoil and turnover in the standards-based open bus realm could spell trouble ahead for the military market. Since the early '90s, when it comes to revenue and development, the military embedded market has had to take a back seat to the commercial market. Back then we had a couple "open systems" buses and a few handfuls of "pseudo open systems" buses. The market for the pseudo open buses was usually driven and controlled by a major system or silicon manufacturer. With the backing of that one large manufacturer, the bus got a sort of built-in critical market mass and could prosper, usually until it was no longer needed or replaced by that manufacturer. During its existence, however, many smaller suppliers would provide a variety of products, filling the various needs of the users.

In contrast, open buses are a little more like a cooperative that may be or has been established by several larger systems or silicon manufacturers. And, in some cases a group of smaller embedded suppliers may modify and spin off an open bus architecture from a proprietary or pseudo bus. A third case might just be a group of companies seeking a technological solution to a set of broad or unique problems. This may all sound like motherhood and apple pie, but it needs to be stated in order to understand why the military market may be in trouble.

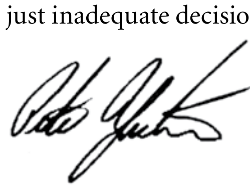
This "buses" thing is a juggling act—one that on occasion works for a while, but eventually the balls start to fall. This juggling act consists of three "balls" in the air at once. First, is a community of suppliers that need one another—while still this is purely for individual gain. Second is a technical issue that needs continual resolution and update. And thirdly, are users with an almost unlimited variation of needs that evolve with time while still requiring ties with the past. Most of the time buses don't get off the ground because the bus doesn't achieve a critical mass in all those three elements. Without achieving a critical mass, the bus lasts as long as the perception that it will achieve critical mass is accepted by the users—in other words, good marketing. When buses fail or die they have limited effect in the commercial marketplace, but for the military market the effects can be devastating.

When a bus architecture that was employed starts to show signs that it will fade it begins a death spiral. Suppliers quickly stop designing new products for that architecture and shift their development funds to up and coming technologies. The time line as to how quick or long the death spiral is depends on how large an installed base there is and how long the architecture has been in place. One that was punched up by a lot of hype in the media, but with limited acceptance by users, will drop from the scenes quickly. One that has enjoyed years of being at critical mass will take years to decline and fade away.

Prior to the emergence of the COTS, military market life was simple. Every five or so years, buses that achieved critical mass would start to peak and something else would be on the horizon to take its place. Embedded suppliers as well as users would start to shift their IP and in-house engineering talent to a new technology—a substantial investment for each organization. The system developer's products would start incorporating the new technology and there was limited intertwining of their shippable products, resulting in limited adverse effects to the ultimate customer.

The military has all the same problems the commercial market has, plus it has a much tighter intertwining of legacy systems along with much longer deployable systems life than the commercial market. The stodgy manner in which the military goes through its design and development cycle has kept it relatively insulated from buses and technology that had a false start and never achieved critical mass. Unknowingly the military has been an enormous asset to the commercial embedded market, through its use of varying established bus technologies it has slowed—and in the case of VME completely nullified—the death spiral for many architectures.

So, where's the problem? This decade has seen an explosion of new architectures and design schemes and the rate of introduction will only increase rather than decrease. Since the vast majority of growth is in the commercial world, the military as a percentage of the total continues to decline. Buses and architectures that don't make it are easily absorbed and forgotten. Military designers are getting younger and are more eager to incorporate the latest and the greatest technology and buses. That's all good as long as someone analyzes the broad picture and is assured that the bus technology they plan to use can continue to juggle all the balls and has longevity. Remember, except for military-specific buses, the military has no input to the juggling. This whole process requires three-dimensional thinking and good management decisions. And when linear thinking along with bad decisions are made, the problems or failures can't be blamed on COTS or open systems. It's just inadequate decision making. ▮▮



Pete Yeatman, Publisher
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The Inside Track

Quantum3D Wearable PC Chosen for Mounted Warrior Demo

Telephonics has selected Quantum3D's Thermite Tactical Visual Computer (TVC) for use in Telephonics' Multi-Media Communications Technology Demonstrator for the U.S. Army Mounted Warrior (MW) Ensemble. The MW Ensemble (Figure 1) is an integrated soldier-fighting system intended to enhance the lethality, battle-command compatibility, survivability, mobility and sustainability of mounted and dismounted Stryker Brigade Combat Team (SBCT) infantry soldiers. When equipped with Multi-Media Communications Technology, the MW Ensemble facilitates the sharing of battlefield multi-media information between soldiers, vehicles and command elements and further integrates individual soldiers into the chain of command by providing interoperability with the digital command and control of other platforms.

The purpose of the MW Multi-Media Technology Demonstrator is to assess the benefits of integration of low-data-rate battlefield video sources including driver enhanced video, FBCB2 data, situational awareness and reconnaissance data and weapons targeting video into a Stryker unit. A key component of the system is the Therrmite TVC, which is optimized for man-wearable, battery-powered applications, and enables dismounted soldiers using software to relay specific multi-media data including video and images via Telephonics TruLink wireless intercommunications system to and from Stryker or other vehicles as well as to other MW Multi-Media Communications-equipped soldiers. The Thermite TVC also enables the video/image data being captured and/or relayed to be displayed on the soldier's monocular HMD monocle or via a handheld LCD available for the MW Ensemble.

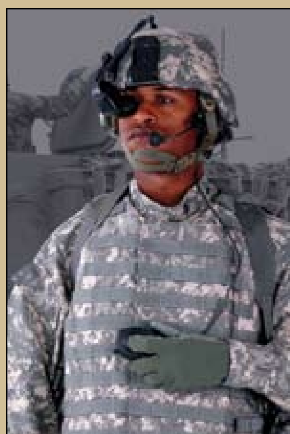

Figure 1

The Mounted Warrior Ensemble is an integrated soldier-fighting system intended to enhance the lethality, battle-command compatibility, survivability, mobility and sustainability of mounted and dismounted Stryker Brigade Combat Team (SBCT) infantry soldiers.

Telephonics
Farmingdale, NY.
(631) 755-7000.
[www.telephonics.com].

Quantum3D
San Jose, CA.
(408) 361-9999.
[www.quantum3d.com].

Northrop Grumman Presents Platinum Source Award to Phoenix International

Phoenix International has received Northrop Grumman's Platinum Source Award, reflecting the Company's sustained excellence as a supplier of quality products and on-time delivery to Northrop Grumman Integrated Systems (IS) Sector. The award was presented to the Phoenix International executive team at the Company's headquarters in Orange, California, by executives from Northrop Grumman Integrated Systems El Segundo, California headquarters. Phoenix International, an ISO 9001:2000-certified manufacturer and Service Disabled Veteran Owned Small Business (SDVOSB), designs and manufactures rugged data storage systems ranging from multi-terabyte Fibre Channel RAID, NAS, SAN and array configurations to Solid State plug-in VME and Compact PCI storage modules.

Phoenix International supplies Northrop Grumman Integrated Systems Sector with high-performance data storage systems used in Joint STARS aircraft as well as in training and support applications. The Platinum Source Award was made in recognition of Phoenix International's demonstrated distinction in meeting performance standards—outstanding quality, commitment to meeting delivery schedules, and focus on customer satisfaction.

Phoenix International
Orange, CA.
(800) 203-4800.
[www.phenxint.com].

L-3 Chooses OSI Geospatial COP System for Navy's DDG 1000 Program

OSI Geospatial will provide its Common Operational Picture (COP) product to L-3 Communications Marine Systems for integration into the bridge system of the DDG 1000 (formerly called DD(X)), the U.S. Navy's next-generation destroyer. OSI's subcontract includes a Linux version of its current COP

Figure 2

Developed under the DD(X) destroyer program, Zumwalt is the lead ship of a class of next-generation multi-mission surface combatants tailored for land attack and littoral dominance with capabilities that defeat current and projected threats and improve battleforce defense. The ship will carry the designation and hull number DDG 1000. The image shown here is an artist's rendering of the DD(X) next-gen destroyer.

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product, plus testing, training and support services.

The integration of the COP product into the bridge systems of the DDG 1000 vessels will deliver enhanced situational awareness and support improved decision-making capability at strategic, operational and tactical levels. Raytheon Integrated Defenses Systems is the prime mission systems equipment integrator for all electronic and combat systems aboard DDG 1000 Zumwalt Class naval destroyers. L-3 Marine Systems was selected by Raytheon to provide the integrated bridge system component for the DDG 1000 program. An integrated bridge system automatically collects, processes, controls and displays vital navigation sensor and control data in order to maximize ship efficiency and safety. OSI will be a third-tier vendor under the program.

OSI Geospatial
North Vancouver, BC
Canada
(604) 904-4627.
[www.osigeospatial.com].

Ultra-DNE Wins $18.4 Million Order from U.S. Marine Corps

Ultra Electronics-DNE Technologies, a manufacturer of tactical voice and data communication systems, announced that the United States Marine Corps (USMC) has placed an $18.4 million order with the company as part of the USMC's AN/MRC-142 Product Improvement Program (PIP). Ultra-DNE will provide high-speed tactical access concentrators and protocol converters to the program, with scheduled deliveries through 2008.

The AN/MRC-142 system is a medium-range, Ultra-High Frequency (UHF) line-of-sight radio system used by the Marines to communicate between deployed troops and Command and Control centers. The AN/MRC-142 PIP replaces obsolete tactical communications equipment, enabling the Marines to access a wider variety of data—such as video and imaging—at faster speeds. The program will improve communications between deployed units at speeds up to eight times faster than the currently fielded systems, improving throughput from 2 Mbits/s to 16 Mbits/s. The new system will now interface with other communications systems, such as the TRC-170 and Transition Switch Module (TSM), which will operate at speeds up to 16 Mbits/s.

The company holds IDIQ contracts with both the U.S. Army (CECOM) and the U.S. Navy (SPAWAR) to provide communications equipment throughout all four branches of the U.S. DoD. Ultra-DNE's sister company, Ultra-TCS, is also providing high-speed line-of-sight radio systems to the AN/MRC-142C improvement program.

Ultra-DNE
Wallingford, CT.
(203) 265-7151.
[www.ultra-dne.com].

Lockheed Martin Selects Aonix PERC VM for Aegis Weapon System

Lockheed Martin has selected the Aonix PERC Ultra virtual machine (VM) for the Aegis Weapon System Open Architecture Program. The Aegis Open Architecture team aims to enhance the capabilities and service life of the U.S. Navy's premier surface combat system while also reducing its cost. Lockheed Martin reportedly selected the Aonix PERC VM based on its ability to provide deterministic, real-time performance and high productivity development.

The Lockheed Martin Aegis team was faced with programming language selection for its Open Architecture Program. Java was selected for several critical subsystems due to its superior tool and library support along with its superior productivity and portability. However, traditional Java offerings could not meet the challenge of the critical timing requirements for the Aegis project. In contrast to its competitors, PERC Ultra, with its deterministic capabilities and ahead-of-time compilation, offered Lockheed Martin the responsiveness it needed to meet its most demanding timing requirements. In addition to real-time threading and deterministic garbage collection, PERC Ultra provided the instrumentation and VM management tools necessary to support the mission-critical real-time requirements of the Aegis Weapon System.

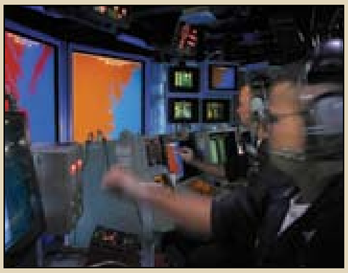

Figure 3

The Aegis Weapon System is a radar and missile system seamlessly integrated with its own command and control system, capable of simultaneous operation defending against advanced air, surface and subsurface threats.

The Lockheed Martin-developed Aegis Weapon System is the world's premier naval defense system and the sea-based element of the United States' Ballistic Missile Defense System. The Aegis Weapon System is a radar and missile system seamlessly integrated with its own command and control system, capable of simultaneous operation defending against advanced air, surface and subsurface threats. Currently, Aegis Weapon System capabilities are on 80 cruisers, destroyers and frigates on station around the world, with more than 25 under construction or planned.

Aonix
San Diego, CA.
(858) 457-2700.
[www.aonix.com].

General Dynamics Selects Virtutech's Tool for NASA GLAST Project

General Dynamics C4 Systems has deployed Virtutech's Simics to develop and test mission-critical embedded flight software for the NASA Gamma-ray Large Area Space Telescope (GLAST) project. Virtutech Simics simulates the spacecraft hardware to create a robust training tool for the GLAST mission operations team to prepare for normal spacecraft operations. By injecting faults in the simulated flight hardware, the mission operations team can implement efficient responses to possible failures or anomalies in the actual system prior to the launch, which provides comprehensive training opportunities and invaluable insight into the activities of the real system long before the actual hardware arrives.

Virtutech Simics provides a virtualized software development environment, minimizing the need to build multiple multi-million-dollar test models of real flight hardware. Using Virtutech Simics, General Dynamics simulates satellite processors and other spacecraft avionics hardware so that the flight software cannot detect the difference from running on real production hardware. With simulation, developers have full control over the code for extensive and thorough testing.

Virtutech
San Jose, CA.
(408) 392-9150.
[www.virtutech.com].

COTS Websites

www.picmg.org

PICMG Site is Ground Zero for cPCI, MicoTCA and More

With an original mission of extending the PCI standard for use in non-traditional computer markets such as industrial automation, medical, military and telecom markets, the PCI Industrial Computer Manufacturers Group (PICMG) has moved way beyond that. With the advent of fabric-based transports, PICMG specs have continued to evolve. This has resulted in a series of specifications that include CompactPCI, ATCA, AMC, CompactPCI Express, MicroTCA, COM Express and SHB Express. Now that many of those have gained some degree of acceptance in defense applications, PICMG ranks as a key consortium for the military market to keep tabs on.

Founded in 1994, PICMG today is a consortium of over 450 companies who collaboratively develop open specifications for high-performance embedded computing applications. The members of the consortium have a long history of developing leading-edge products for these industries. Each specification has a unique PICMG identifier. And the PICMG Web site provides details on each specification, including those under development, in its Specifications Directory. These specifications are represented by many leading-edge products from PICMG member companies, details of which can be found in our Product Directory. A members-only portion of the Web site provides enhanced access to information and ways to participate in the consortium's activities.

PICMG
Wakefield, MA.
(781) 246-9318.
[www.picmg.org].

FPGA Tech Advances Propel Software Radio Forward

Advances in FPGA density, speed and DSP capabilities are enabling portable software radio designs that can meet the size, weight and power needs of tactical radios.

Jeff Child
Editor-in-Chief

For a variety of military applications, FPGAs have become a core enabling technology—as critical as processors, memory and I/O interface silicon. But no segment is perhaps so dependent on advances in FPGAs than Software Defined Radio. While first-generation software radios used a mix of ASICs, FPGAs, digital signal processors (DSPs) and general-purpose processors, the trend now is toward relying mostly on FPGAs. Advances in FPGAs—in gate density, speed, and in digital signal processor architectural enhancements, have been a huge boon to the development of SDR technology. FPGAs in particular are critical in handheld/manpack varieties of software radios where size, weight and power concerns are a gaining factor. System designers are relying on advanced FPGA devices like the Virtex-4 and Virtex-5 family from Xilinx, and Altera offers low-power solutions through its MAX II, Cyclone II and HardCopy II device families.

Embedded board vendors are keeping pace with board-level FPGA-based solutions. An example, released earlier this year, is a pair of boards from VMETRO designed around the Xilinx-5 family of FPGAs. The products, based on open standard form-factors including PMC and PCI (Figure 1), are targeted for deployed embedded applications as well as development platforms. For PCI-based development platforms, VMETRO's DEV-FPGA05, based on the Xilinx LX50 Virtex-5 FPGA, will be bundled with a software support package to allow Virtex-5 applications to be evaluated and developed at low cost. For deeply embedded applications, the PMC-FPGA05 PMC module with a Virtex-5 LX110 is available.

Figure 1

Useful for development work or deployed software defined radio systems, these two boards—one PCI, one PMC—from VMETRO are based on the Xilinx LX50 Virtex-5 FPGA and Virtex-5 LX110.

Reusing and Porting Waveforms

SDR provides an efficient and low-cost solution to the problem of building multifunctional, multimode, multiband, wireless devices that can be enhanced via software upgrades. SDRs also allow the reuse of waveform code from platform to platform, which requires a software infrastructure supporting code portability. That capability is critical for the DoD's Joint Tactical Radio System (JTRS) program that mandates future radios become interoperable with one another and support the different waveforms across the Armed Forces branches. SDR technology also eases the chore of porting applications to future hardware. That's a big

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The Joint Tactical Radio System: Reorganized and Rescoped

After nearly a year on hold, the DoD's Joint Tactical Radio System (JTRS) program went back in motion earlier this year, after a significant management restructuring and rescoping of the program. First off, the various Clusters that make up JTRS were renamed. The Army's portion of the JTRS program is to be known as "JTRS Ground Systems." Cluster 1 becomes "Ground Mobile Radio," while Cluster 5 will be known as "Handheld/Manpack/Small Form Fit (HMS) radios. Meanwhile, Cluster AMF separates into AMF Small Airborne (AMF-SA) and AMF Maritime (AMF-M). Table 1 lists the domains of the restructured JTRS program.

JTRS Domain Descriptions	
Ground Domain	Ground Mobile Radio (GMR) (formerly Cluster 1) - Support requirements for Army and Marine Corps Ground Vehicular platforms. Handheld/ Manpack/Small Form Factor (HMS) (formerly Cluster 5) - Support requirements for JTRS handheld and manpack units and forms suitable for integration into platforms requiring a Small Form Fit radio
Airborne, Maritime and Fixed Domain	Airborne, Maritime and Fixed Site (AMF) - Support requirements for airborne (including rotary wing), maritime and fixed station platforms for all Services. Multifunctional Information Distribution System–JTRS (MIDS-J) - Migrate the current MIDS-Low Volume Terminal to MIDS-JTRS compliance producing the next-generation data link and communication terminal for joint and coalition tactical platforms
Network Enterprise Domain	Waveform Program Office - Responsible for waveform development, cryptographic equipment applications, architectural integrity of JTRS, gateways and common network services
Special Radio Systems	JTRS Enhanced Multi-Band, Inter/Intra Team Radio (MBITR) (formerly Cluster 2) - Managed by Special Operations Command. Supports requirements for handheld radios for the Army, Navy, Marine Corps and Air Force Special Operations Forces

Table 1

Described here are the various domains that encompass the restructured JTRS program.

Beyond those name changes, the biggest change in JTRS is a dramatic paring back in the number of waveforms to be included. In the initial ORD there were 32 waveforms—many of which were key to interoperability with legacy radios. The reorg—under ORD 3.2.1—reduces that list of waveforms down to six. They haven't ruled out doing all 32 at some point, but the goal now is to focus on six. The six include WNW, SRW, SINCGARS, EPLRS, MUOS and Link-16. What that suggests is a focus on empowering the networked battlespace—Soldier Radio Waveform (SRW) and Wideband Networking Waveform are the two networking waveforms. Meanwhile, only limited backward compatibility with old radios—SINCGARS and EPLRS waveforms—is included. MUOS and Link-16 are included for the airborne form-factors. Satellites supporting MUOS haven't been launched yet, but are expected to be in the next year or so.

deal for the defense sector where applications can be deployed for a long period of time, extending beyond the lifetime of the hardware.

While the deployment phase for JTRS is still years away, the military nonetheless is making a shift to software radios. In a recent example, Harris, a major supplier of software defined tactical radios, was awarded a $1.9 million contract from the U.S. Navy Expeditionary Combat Command (NECC) for Falcon III AN/PRC-152(C) multiband handheld radios. The radios will be deployed to satisfy the U.S. Navy's urgent operational requirement to support Explosive Ordnance Disposal (EOD) and Naval Coastal Warfare Group operations in Iraq and Afghanistan.

The Harris AN/PRC-152(C) is a next-generation, multiband handheld radio that offers military users advanced capabilities for critical operational requirements. The AN/PRC-152(C) is the first NSA-certified radio to implement the government's Software Communications Architecture (SCA). SCA is the software architecture mandated in the JTRS program radios. ▮

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VMETRO
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[www.xilinx.com].

Main Feature

FPGAs for Software Radio

FPGAs Muster Up Solutions for Software Radio

Timing, data formatting, digital conversion, DSP—the list of software radio duties suited for today's crop of FPGAs continues to grow, elevating them to the role of the enabling technology for military software radio designers.

Rodger Hosking, Vice President
Pentek

Software defined radio technology has been widely adopted for new military and aerospace platforms, government signal intelligence and homeland security systems, and now more extensively in commercial wireless voice and data networks. Most of these communication systems employ digital signaling, and as signal bandwidth increases to handle more video, voice and data traffic, the sampling rates increase accordingly. The need to squeeze more channels of traffic into an expensive slice of precious radio spectrum has led to advanced code modulation schemes such as CDMA and its more complex derivatives.

Government requirements for secure communications mandate real-time encryption and decryption schemes that must be increasingly more resistant to interception. Multinational theater of war combat operations must selectively ensure certain specific communication links and reliably deny others. All of these factors drive the need for faster, flexible and more powerful DSP processing resources.

FPGAs and Software Radio: A Winning Team

For many years, hardware design engineers have taken advantage of FPGAs for connecting high-speed software radio peripherals like wideband A/D and D/A converters, digital receivers and communication links to programmable processors in embedded real-time systems. Figure 1 shows an example software radio from Rockwell Collins, one of the producers of the first Joint Tactical Radio System (JTRS)-compliant software defined radio communications system for the U.S. Army.

FPGAs are especially well suited to handle the clocking, synchronization, and other diverse timing circuitry needed to tame these specialized devices. In addition, FPGAs are excellent for data formatting tasks like serial-to-parallel conversion, data packing, time stamping, multiplexing and packet formation.

With shrinking die geometries and other advances in chip technology, FPGA silicon became much faster and denser. But more importantly, the addition of new high-performance DSP resources marked a watershed event that dramatically changed the architectural paradigm of software radio systems. FPGAs are now incorporated in software radio products primarily for their digital signal processing engines, thus stealing the spotlight from the more mundane traditional roles that they still serve admirably.

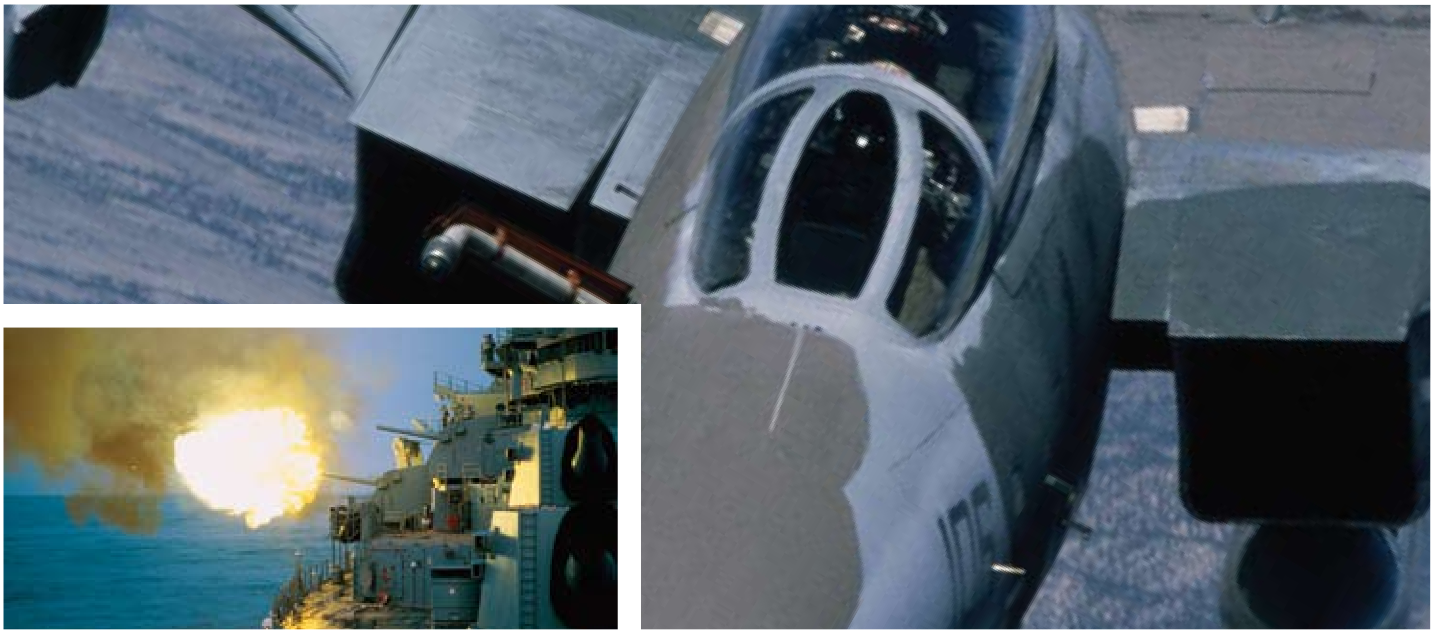
Third-Gen DSP Blocks

Without exception, the latest device offerings from major FPGA vendors offer second- or third-generation DSP blocks. They include extended precision multiplier/accumulators, advanced arithmetic units, logic engines and flexible memory structures that can be tailored into block memory, dual-port RAM, FIFO memory and shift registers.

While these DSP capabilities of new FPGAs are truly remarkable, several other significant features add even more benefits to software radio applications.

Figure 1

FPGAs are ideal for connecting high-speed software radio peripherals like wideband A/D and D/A converters, digital receivers and communication links to programmable processors in embedded real-time systems. Shown here are some example software radios from Rockwell Collins, one of the producers of the first Joint Tactical Radio System (JTRS)-compliant software defined radio communications system for the U.S. Army. The top image is a prototype of a JTRS Airborne radio, the bottom image is a prototype of a JTRS Ground radio.



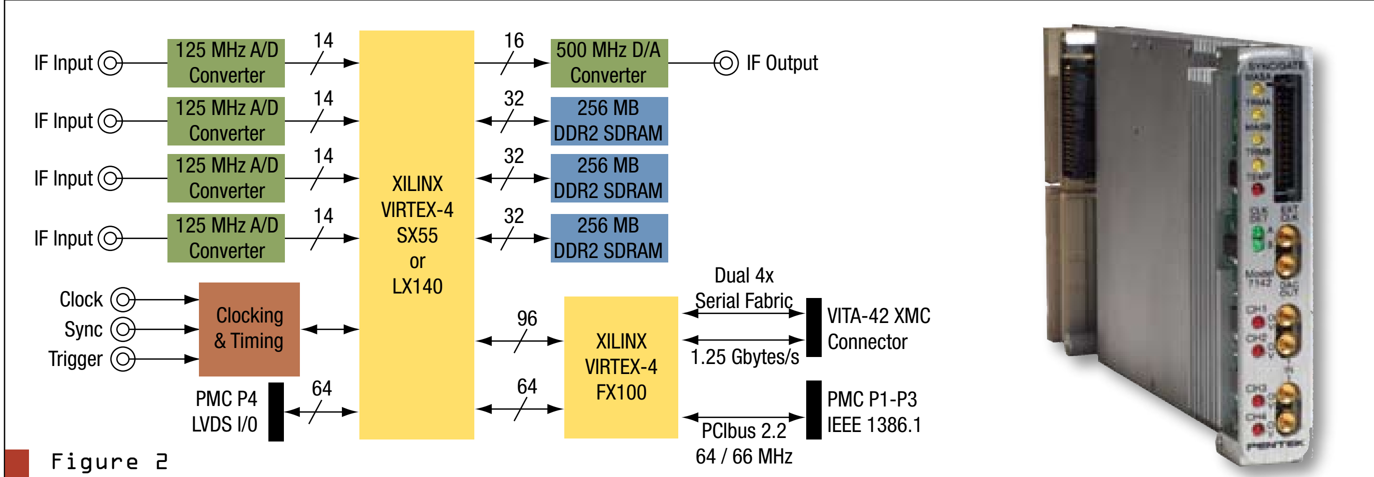


Figure 2

An example platform solution targeting software radio designs is Pentek's Model 7142 PMC module. Real-time DSP tasks such as digital up- and down-conversion, modulation and demodulation, encoding and decoding, and other operations on the board are performed using FPGA-based DSP resources.

Onboard serial gigabit transceivers and channel coding/decoding engines support the emerging switched serial fabric protocols that are quickly replacing conventional parallel buses and backplanes for high-speed inter-chip and inter-board data transfers.

Other new features include onboard programmable RISC processors that can execute code for local supervision and control functions, thus greatly reducing the need for an external host processor. These processors slash loop latencies to deliver much tighter real-time control systems. Finally, Ethernet MACs (media access controllers), incorporated as I/O resources for the latest-generation FPGAs, simplify TCP/IP communication links to a wide range of host processors and various operating systems.

Uses for FPGA Resources in Software Radio Systems	
✔	Interfacing to ASICs including A/Ds and D/As
✔	Digital down-converters (DDCs) and digital up-converters (DUCs)
✔	Modulating and demodulating for precise frequency spectrum utilization
✔	Encoding and decoding for complex multichannel standards
✔	Encryption and decryption for secure communication
✔	Signal identification and tracking using FFTs and adaptive control loops
✔	Receive and transmit beamforming for directional control and signal enhancement
✔	High-speed interconnects between devices and between system components
✔	Localized high-level control using onboard processors for autonomous operation
✔	Simplified communication to host networks using onboard Ethernet MACs

Table 1

The current crop of FPGAs provides useful connectivity and processing resources for software radio. Listed here are ten key ways that FPGA resources offer a direct benefit for such systems.

New FPGA Device Examples

Competition for design wins is stronger than ever, leading to an exciting race among FPGA vendors for features that deliver maximum performance and specific benefits. Winning this race, however, is a complex and elusive goal. With so many different types of resources—block RAM, distributed RAM, DSP blocks, logic blocks, microcontrollers, gigabit ports, I/O drivers and pins and so on—balancing a single optimum ratio is futile because each application requires a different blend. For example, the design engineer selecting the best part for a logic-intensive application will avoid an FPGA heavily burdened in cost and power with a wealth of powerful DSP blocks. As a compromise, vendors have developed multipronged product offerings, each targeting different classes of applications.

One example of such a family is the Xilinx Virtex-4 FPGA. Unlike the previous Virtex-II Pro family, Xilinx has split the seventeen Virtex-4 product offerings into three subfamilies, each emphasizing distinct strengths. For the recently announced Virtex-5 family, there are a total of four distinct subfamilies, but detailed information on only the first of these has been made public to date.

The Virtex-4 uses a 90 nm process and a core voltage of 1.2V, while the Virtex-5 shrinks the feature size down to 65 nm and drops the core voltage down to 1V. This allows an improvement in maximum clock speed to 500 and 550 MHz, respectively, while reducing power consumption.

Logic Building Blocks

Configurable Logic Blocks (CLBs) are the basic elements used for implementing state machines, combinatorial logic, controllers and sequential circuits. They are composed of logic "slices" with flip-flops, look-up tables (LUTs), multiplexers, Boolean logic blocks and adder/subtractors with carry-look-ahead functions. The Virtex-5 uses 6-input LUTs instead of the 4-input LUTs in the Virtex-4, providing additional logic functions, fewer levels of logic for faster speed and less power due to simpler routing.

Twenty different user-configurable interface standards for the device I/O pins offer flexible connections to a diverse range of external hardware devices. New in the Virtex-4 and continued in the Virtex-5 is the active termination feature that not only provides programmable termination within the FPGA to drastically reduce the number of external discrete resistors, but also dynamically adjusts termination impedance to track changes in drive levels due to process, temperature and device variations.

Source-synchronous interfaces include serializer/deserializer blocks that match faster data rates on external data buses to slower, wider buses inside the FPGA to help reduce power. Interfaces to a wealth of fast external memory devices include DDR and DDR2 SDRAM, QDR and QDR II SRAM and RLDRAM II. These interfaces are made easier with programmable clock and data skew circuitry to match complex setup and hold time requirements.

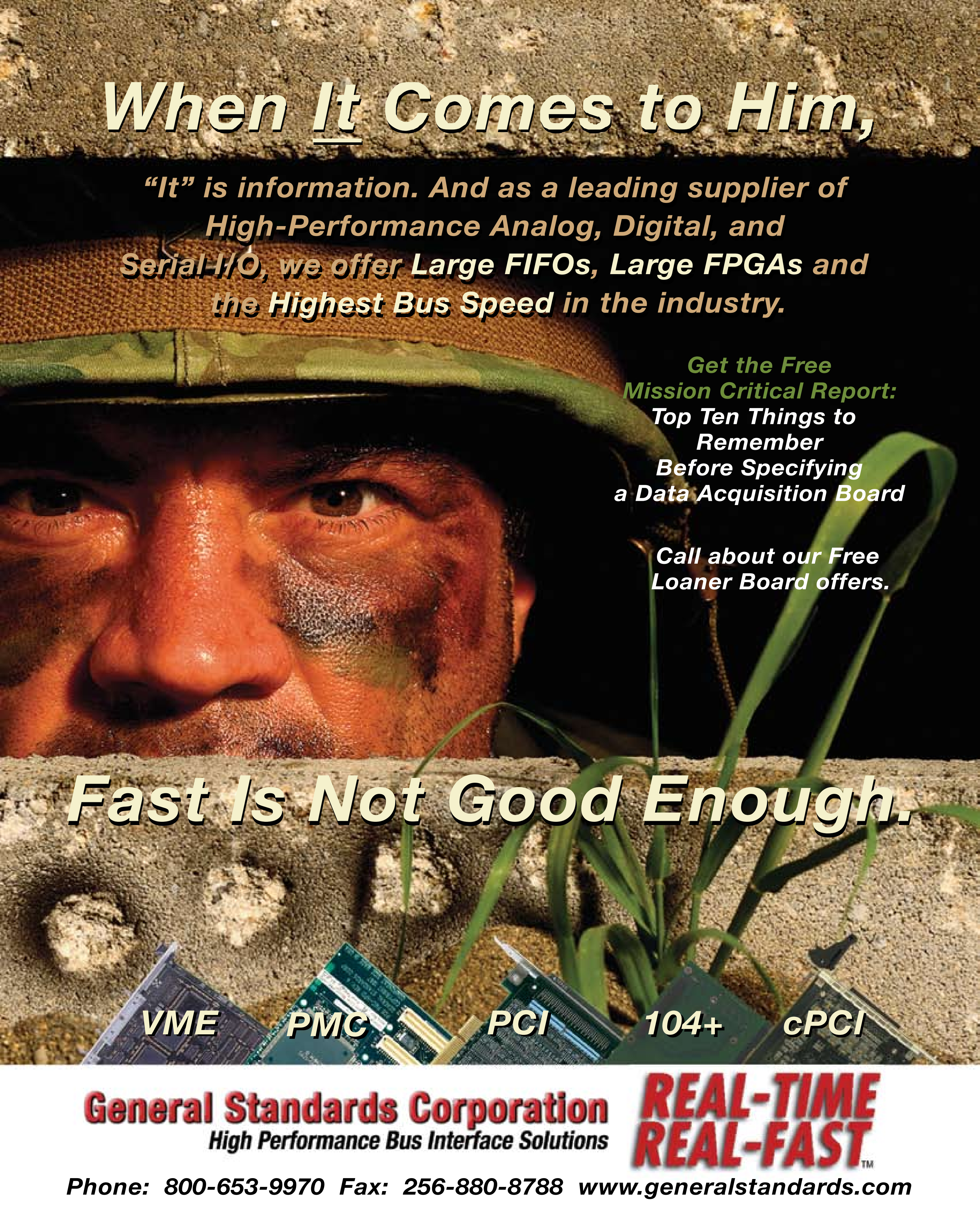
Digital clock managers allow different regions of the FPGA to be operated at different clock frequencies that can be synchronized from various external clock references. Frequency synthesizers with multipliers and phased-matched clock dividers precisely align external timing signals with data sources and destinations.

Different Mixes of Resources

All of the resources described so far are available in all Virtex-4 and Virtex-5 devices, but the ratio of these resources differs significantly among the subfamilies. The LX subfamilies for the Virtex-4 and Virtex-5 deliver the most logic and I/O. The Virtex-4 SX subfamily aims at DSP with 512 XtremeDSP slices, and the FX subfamily offers generous memory and three other important resources found only in FX devices. The first of these are onboard IBM 405 PowerPC processor cores that can be used as local microcontrollers to implement complete systems on a chip, often eliminating the need for an external CPU for high-level supervisory functions.

The second resource is a set of serial gigabit transceivers capable of handling bit rates up to 10 GHz and backed up with serializer/deserializer logic. By configuring these interfaces through available IP cores, the FPGA supports popular high-speed serial standards and switched serial fabrics including Serial RapidIO, PCI Express, Fibre-Channel, SATA, SONET, and many others.

The third resource unique to the FX family is a set of 802.3-compliant Ethernet media access controllers (MACs). These support 10/100/1000 Base-x transmit/receive interfaces to system peripherals, and are especially useful to the embedded PowerPC processors as a standard communication link to the outside world. While no Virtex-5 subfamilies beyond the LX devices have been announced at this time, it is logical to expect that enhanced versions of these last three resources will be found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on at least some of the future subfamily offerings. Table 1 lists ten key ways that FPGA resources offer a direct benefit for software radio systems.

Software Radio Product Example

Harnessing these resources for a high-performance software radio product illustrates the usefulness of the subfamily differentiation. The product shown in Figure 2 is the Model 7142 PMC module suitable for use in many different types of embedded computer systems, including PCI, VME and CompactPCI card cages. The new XMC extension to PMC defined by VITA 42 offers Gbit serial links supporting the new popular switched fabric protocols.

Four 125 MHz 14-bit A/D converters and one 500 MHz 16-bit D/A converter provide analog IF (intermediate frequency) signal interfaces to external analog RF up- and down-converters and RF amplifiers for ultimate connection to the antenna. Real-time digital signal processing tasks such as digital up- and down-conversion, modulation and demodulation, encoding and decoding, and other operations are often all performed using FPGA-based DSP resources.

As a PMC module, a PCIbus interface must be provided along with DMA controllers and FIFO buffers to move data efficiently between the PCI bus and the many peripherals on the module. As an XMC module, the unit must include gigabit serial transceivers and some facility for implementing a serial fabric and/or protocol.

Delivery of the Model 7142 was required prior to Virtex-5 device availability, so the Virtex-4 family was chosen to meet the module requirements. Since only the versatile FX subfamily provided all of the necessary features, it becomes an obvious choice for this product. Nevertheless, the FX family is quite limited in DSP capability compared to the SX family. Even the largest member of the FX family has only the same number of XtremeDSP slices as one of the smaller SX devices. Since customer access to ample DSP horsepower was a critical factor, an SX55 device was added to the PMC module, significantly boosting the total quantity of DSP slices from 192 to 704.

Because software radio technology drives such a diverse array of commercial, industrial, military and government electronic systems, the new features and inherent flexibility afforded by FPGAs deliver an excellent solution. The increasing quality and quantity of IP core offerings for highly optimized algorithms, interfaces and protocols help embedded board vendors shorten their time-to-market, and help systems integrators add critical functions to these FPGA-based products for specialized turnkey applications. EDA tool vendors race to digest and tame the increasing complexity of these new hardware offerings, and compete with each other in reducing design time, improving design integrity, and maintaining portability to next-generation devices.

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Main Feature

FPGAs for Software Radio

FPGAs Cater to a Diverse Set of Military Needs

FPGAs are becoming essential building blocks in the implementation of many diverse military applications. Meeting the broad and unique demands of the military market is a challenge for FPGA vendors.

Amr El-Ashmawi, Strategic Customer Manager
Military/Aerospace Business Unit, Altera

Military applications where programmable logic is key span a diverse range, including handheld radios, heads-up displays, battlefield sensors, unmanned air and ground systems, multi-function radar and electronic warfare systems, tactical and strategic missiles. They are also used in large aircraft with subsystems such as electronic warfare, radar and communications. All these widely differing applications have fundamental requirements based on the functions and operational environment of the electronics system. As a result, the military electronics sector can't be viewed as a single sector, but rather many with some important things in common.

No one family of FPGAs can fit all military contractors' design needs. The range of requirements is very broad. Suppliers can cater to one specific segment with a single product offering, but what is desired by prime DoD contractors is a diverse offering of FPGAs meeting the requirements for a range of military applications. The mix should include high-density, high-performance devices as well as low-cost, low-power devices. Meanwhile, combining varying device types with a structured ASIC that provides a manufacturing path from design-to-production process reinforces the value this market segment requires. Using structured ASICs in production volumes can add another level of robustness while reducing cost, lowering power requirements, adding security to mitigate IP tampering, as well as increasing performance.

Software Radio Requirements

Take for example the challenges in designing programmable logic into handheld, combat radios. These systems merge the needs for high-speed, multi-waveform processing while operating on a single battery charge with 48-hour operation requirement. An FPGA able to process numerous waveforms such as Soldier Radio Waveform (SRW) and Wideband Networked Waveform (WNW) is required, but it must also be able to manage the low power requirements of the application as well as be cost-effective at projected system volumes.

The right FPGA for the task must be sensitive to power requirements since it is

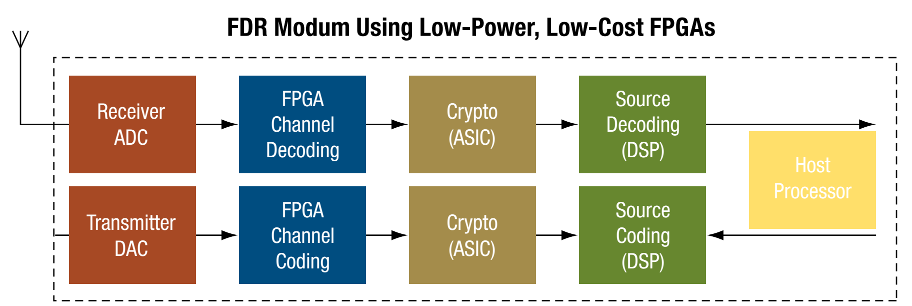

Figure 1

Because most military software radios are battery powered, FPGAs must be sensitive to power requirements. They must also be cost-sensitive since military radios are needed in relatively high volumes. Shown here is an example of a software defined radio design using low-cost, low-power FPGAs.

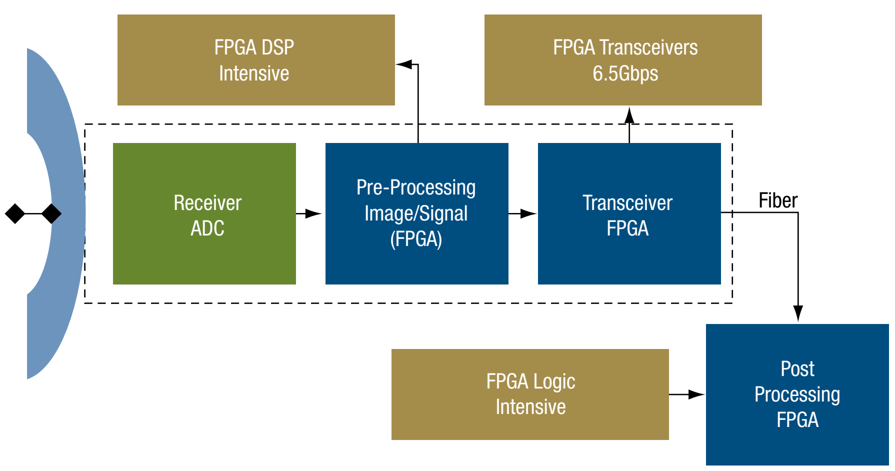

Figure 2

In military radar systems, the trend is toward moving processing closer to the radar antenna where pre-processing and high speed on-chip processing of the data signal is required. Implementing both on a single device could increase the risk of device failure. Partitioning tasks in two different devices ensures lower risk for thermal dissipation and flexibility. Today's FPGAs provide DSP capabilities plus high-speed I/Os capable of 6 Gbits.

battery powered. It must also be cost-sensitive since military radios are needed in relatively high volumes. Figure 1 shows an example of a software defined radio design using low-cost, low-power FPGAs.

While low-cost, low-power FPGAs fit the military software radio market segment, that class of device is limited in processing and performance for other military applications such as radar, imaging systems, ballistic Aegis systems and strategic missile systems. Those applications require a full-featured device with prodigious digital processing power and high density allowing execution of large, complex algorithms. The requirements for signal processing in pre-processing (next to the antenna) and post-processing (for rapid reaction) combat the information requirements. Arrays of high-performance FPGAs, employing embedded transceivers that allow data on and off the device quickly, are often used in these sophisticated applications.

Focus on DSP

Radar systems demand large amounts of DSP power supplied by FPGAs, especially when used in target tracking and designation. These systems provide position and velocity with respect to the radar unit. In some advanced systems it is even possible to determine the shape of the object being tracked. The military requires all-weather, day-and-night imaging sensors for supplying reconnaissance, surveillance and targeting information.

Current design efforts bring the processing closer to the radar antenna where pre-processing and high-speed on-chip processing of the data signal is required. Implementing both on a single device could increase the risk of device failure. Partitioning tasks in two different devices ensures lower risk for thermal dissipation and flexibility. Today's FPGAs provide the military systems designer with DSP capabilities plus high-speed I/Os capable of 6 Gbits per second. Figure 2 shows a block diagram of a military radar system based on high-density FPGAs.

In electronic warfare, the military must suppress enemy air defenses to accomplish its objectives and survive. The military achieves this by using specialized

Critical Requirements for Military FPGA Users

✔	A reliable supply chain
✔	State-of-the-art packaging
✔	Device offerings for multiple market segments
✔	Military temperature support
✔	Die business support
✔	Timely product EOL notifications
✔	Obsolescence protection
✔	Anti-tampering design security

Table 1

As FPGAs become ever more critical for military system designers, chip suppliers must meet a complex set of needs particular to the defense market.

aircraft to neutralize, destroy, or temporarily degrade enemy air defense systems by either physical attack or electronic warfare (EW). Specially equipped aircraft temporarily suppress enemy air defenses by transmitting electronic signals that disrupt enemy radar and communications.

Other specialized aircraft use anti-radiation missiles that hone in on enemy radar that supports surface-to-air missiles and anti-aircraft artillery systems by physically degrading or destroying them. FPGAs are used in these specialized airborne systems to provide essential processing power for these demanding situations. These FPGAs also include software productivity tools to help ensure production schedules for the applications are met. A methodology of reuse also ensures military algorithms previously developed can be effectively reused, resulting in significant cost savings.

Unique Demands of Military FPGA Users

Because military prime contractors have essentially a single customer—the Defense Department—they face clearly different electronics purchasing and application design requirements from the commercial sector. Among the challenges military contractors face is acquiring mil-grade FPGAs from an industry where the main emphasis is decidedly not military applications. In fact, the military represents less than 1 percent of North American semiconductor sales. As a consequence, the military does not have much leverage with FPGA vendors to address its specific needs. These needs include eliminating the risk of device failure or underperformance in harsh operating environments, highlighting reliability and productivity concerns, security and device lifecycle questions, and overall access to technology to maintain operational advantages over potential opponents.

Reliable service in extremely demanding operational environments typically requires operational specifications between -55° to 125°C, in high altitude, high and low humidity, during extreme vibration and shock, and in potentially corrosive conditions. Another aspect of reliability is device packaging. The commercial market is racing toward environmentally friendly lead-free packaging. However, using RoHS-compliant devices can adversely affect device reliability in some military applications. Additionally, extended end-of-life (EOL) solutions are needed for military applications with 10-plus years of product use desired. Comparatively, the shelf life of most commercial devices is only 2-3 years. Military contractors need a significantly improved solution over any commercial supply scenario. Table 1 lists the essential needs particular to military users of FPGAs.

FPGA vendors must engage and address more recent criteria developed by the Aerospace Qualified Electronics Components (AQEC) working group. They have produced the GEIA-STD-0002-01 standard, scheduled for release in the near future. FPGA vendors must apply the GEIA standard as part of an approach that provides military industry access to products at an acceptable cost while addressing the added requirements listed above. Clearly, going well beyond traditional commercial-grade requirements should be the future direction. ▮

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DSP Pipeline Scheme Enhances FPGA System Performance

Getting the most out of an FPGA-based military system design is no straightforward matter. Using a DSP pipelined system architecture helps exploit the full capabilties of today's FPGAs.

Ramon Mitchell, Principal Engineer
Radstone Embedded Computing

Many defense and aerospace applications require advanced imaging, multi-sensor processing, sensor fusion and software defined communications platforms. Ideally, this functionality must be deployed quickly with enough built-in flexibility to anticipate the integration of new features over the lifetime of the platform.

This is especially true for rugged embedded platforms that are subject to extensive environmental qualification prior to deployment. These systems must adapt to changing threat scenarios over a ten-year or longer service period with minimal requalification effort during that time.

General-purpose computing architectures offer high levels of reconfigurability but may struggle to keep pace with the computationally intensive nature of these applications. Today, system architects can use a more hardware-oriented approach

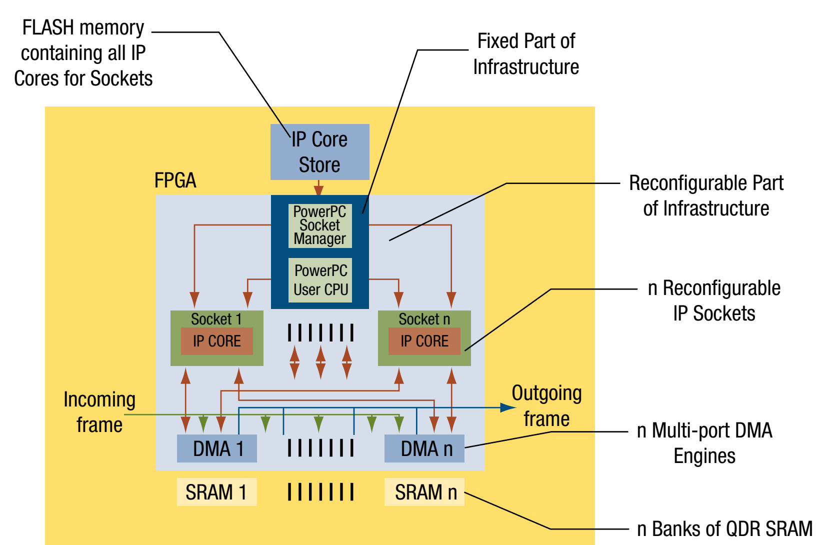
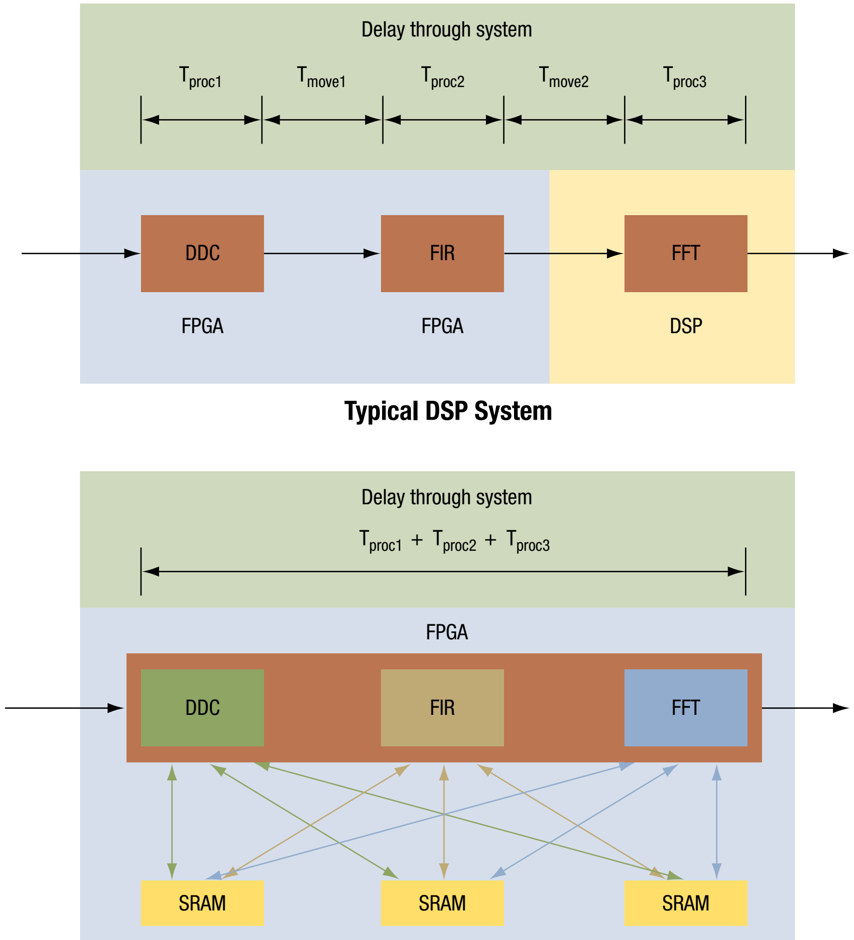


Figure 1

System solutions like this example make FPGA technology accessible to developers who are not familiar with the intricacies of FPGA programming. Here, a preconfigured "pipelined DSP FPGA processor" is programmed using familiar software programming tools using an infrastructure built around an embedded PowerPC system encompassing two embedded processors and a number of "IP.sockets" loaded with one of a selection of FPGA-optimized DSP algorithms.



FPGA Reconfigurable DSP Pipeline

Figure 2

In this typical DSP system made up from FPGA devices and DSP processors, the time taken for data to propagate through the system is made up of processing time (Tproc) and time taken to move data from one node to another (Tmove).

by integrating leading-edge FPGAs with high-performance CPUs to handle high data throughput and tight performance budgets while preserving the ability to improve functionality over time.

FPGA technology is capable of performance boosts for certain types of data processing, which are orders of magnitude beyond those possible from general-purpose processors. It's no wonder that systems designers throughout the military and aerospace market are looking to FPGA technology as the silver bullet that will make all things possible.

Roadblocks to FPGA Adoption

But if adoption of FPGA technology is not yet as widespread as might be expected, there are good reasons. To really leverage the power and capability of an FPGA, three distinct skill sets are required. The first is the domain expert—the source of knowledge about the application, and the problem to be solved. The second is the mathematician—the source of expertise in developing and delivering fast, efficient algorithms. And the third is the FPGA expert—the source of the understanding it takes to translate the requirement and the algorithm

Pipelined DSP Implementation Using FPGAs

The diagrams shown here illustrate how the FPGA reconfigurable DSP pipeline could be used to maximize system throughput in a typical DSP-oriented scenario. The example shows an IP support infrastructure with two IP sockets and three memory banks. During each of the frame times shown, four simultaneous operations are performed at once.

Frame Time 1

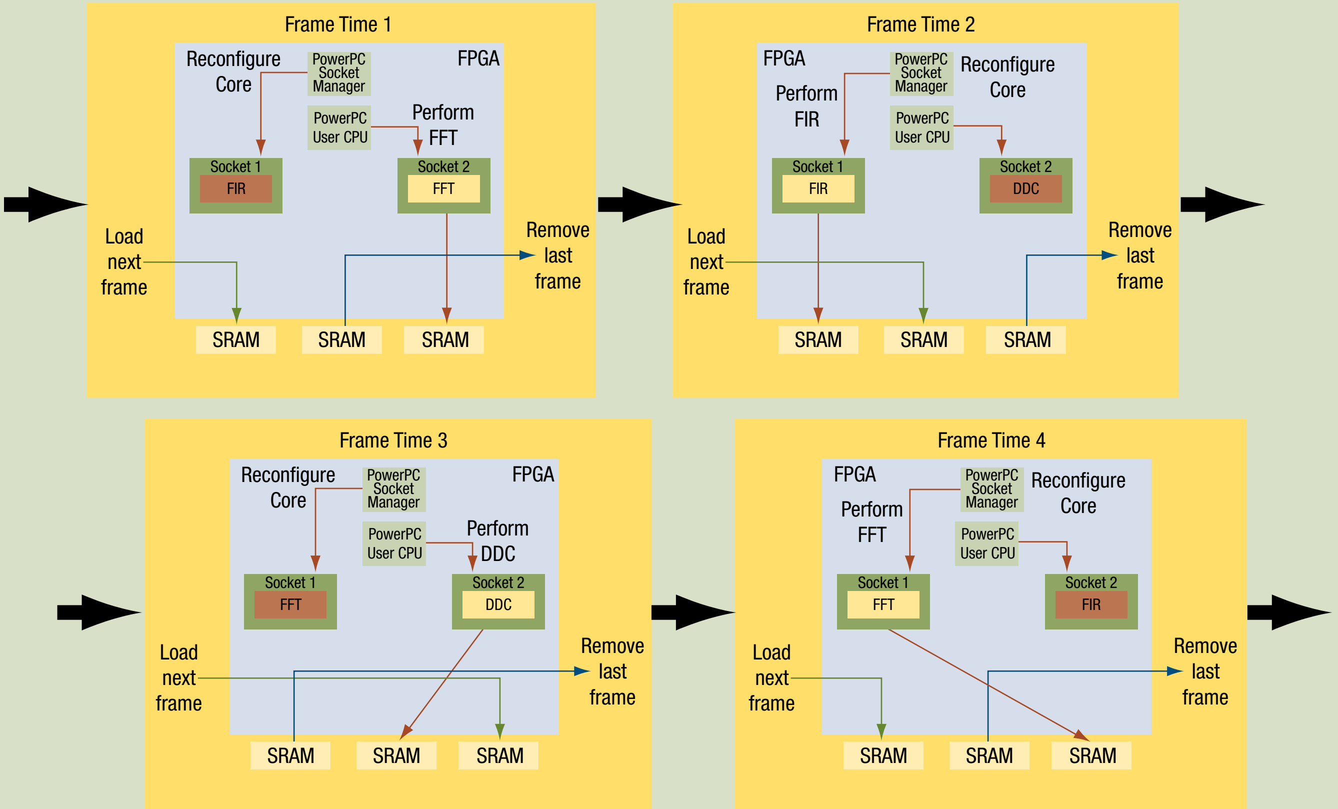
In frame time 1 it has been assumed that data has been preloaded into one bank of SRAM and that the previous frame time has completed its operation on the data in another SRAM bank. The following four operations are performed simultaneously:

1. The next frame of data can be transferred using a dedicated DMA engine from its source into a free bank of SRAM.
2. The last frame of data on which all the pipelined operations have been performed can be transferred out using a dedicated DMA engine to its destination.
3. Socket 1 is being re-loaded with a new IP core to provide FIR functionality.
4. Socket 2 is running an FFT algorithm on a previously loaded frame in a separate SRAM bank, under the control of the user CPU.

Frame Time 2

The following four operations are performed simultaneously:

1. The next frame of data can be transferred using a dedicated DMA engine from its source into a free bank of SRAM.
2. The last frame of data on which all the pipelined operations have been performed can be transferred out using a dedicated DMA engine to its destination.
3. Socket 1 is running an FIR algorithm on the frame loaded in frame time 1, under the control of the user CPU.
4. Socket 2 is being re-loaded with a new IP core to provide DDC functionality.



Figure

Shown here is an IP support infrastructure with two IP sockets and three memory banks. During each of the frame times shown four simultaneous operations are performed at once.

Frame Time 3

The following four operations are performed simultaneously:

1. The next frame of data can be transferred using a dedicated DMA engine from its source into a free bank of SRAM.
2. The last frame of data on which all the pipelined operations have been performed can be transferred out using a dedicated DMA engine to its destination.
3. Socket 1 is being re-loaded with a new IP core to provide FFT functionality.
4. Socket 2 is running a DDC algorithm on the frame loaded in frame time 2, under the control of the user CPU.

Frame Time 4

The following four operations are performed simultaneously:

1. The next frame of data can be transferred using a dedicated DMA engine from its source into a free bank of SRAM.
2. The last frame of data on which all the pipelined operations have been performed can be transferred out using a dedicated DMA engine to its destination.
3. Socket 1 is running an FFT algorithm on the frame loaded in frame time 3, under the control of the user CPU.
4. Socket 2 is being re-loaded with a new IP core to provide FIR functionality.

One of the key benefits of this approach is that multiple tasks can be performed simultaneously. One of the inherent problems with using FPGA technology in a heterogeneous system is the issue of streaming the dataflow from different parts of the system without wasting valuable processing time. This architecture allows data streaming both in and out of the FPGA while maintaining the ability to operate on pre-loaded data at full speed. This is possible because of the support provided by the FPGA embedded processors, which when linking with dedicated DMA engines provide an excellent resource for traffic/data management. In this way it is possible to avoid the typical processor bus bottleneck that encumbers so many alternative architectures.

into something the FPGA can execute at maximum speed.

It goes without saying that those three skill sets rarely, if ever, exist in the same individual. Moreover, the interaction between what are likely to be three experts in translating the problem into the solution is likely to be inherently inefficient and cumbersome.

For the industry to truly derive the full benefit from the potential of FPGA technology and still be able to deliver timely solutions, a way needs to be found of easily harnessing what FPGA silicon can do—a way that ideally, if theoretically, would allow the domain expert to, in effect, create an effective, efficient system without needing recourse to either the mathematician or the FPGA guru.

So what are the alternatives? The way things stand, the tools exist that would enable, for example, the FFT to be easily executed on a PowerPC. The problem is, the PowerPC lacks the necessary horsepower. The FPGA has the requisite horsepower—but putting in place the infrastructure necessary to enable it to run is, today, an inordinately complex and time-consuming process. What is needed are system solutions—beyond those that are routinely provided by the FPGA vendors, and beyond even the software development kits that FPGA resellers typically deliver—that make the power of FPGA technology accessible to developers who are not familiar with the intricacies of FPGA programming.

FPGA Reconfigurable DSP Pipeline

One possible approach is a preconfigured "pipelined DSP FPGA processor" that is programmed using familiar software programming tools and requires little detailed knowledge of FPGA design fundamentals. The block diagram in Figure 1 illustrates what this might look like.

The FPGA reconfigurable DSP pipeline would comprise a preconfigured IP support infrastructure. The infrastructure would be built around an embedded PowerPC system encompassing two embedded processors and a number of "IP sockets," which can be loaded with one of a selection of FPGA-optimized DSP algorithms. This is done using partial reconfiguration techniques, under the control of the socket manager, implemented using one of the embedded PowerPC processor cores. Each socket can be loaded independently without affecting the run-time operation of the other sockets or the rest of the FPGA. The other PowerPC processor core would be available to the application software to control and manage the overall application.

Each IP support infrastructure would support multiple memory banks. Each memory bank can be accessed by all the sockets through a multi-port

DMA memory controller, facilitating simultaneous operation of all memory banks and allowing one bank to load the next frame of data; a second bank to read out the last frame of data; and the remaining banks to be operated on by the algorithms loaded into the IP sockets.

A range of IP support infrastructures would be available that would allow the use of a small number of larger IP sockets or a larger number of smaller IP sockets. The memory banks may also be configured to assign multiple banks to IP sockets requiring larger frame sizes.

Part of each of these infrastructures would be dedicated to managing dataflow. This would be done under the control of the user CPU, but actually managed by the socket manager. The socket manager would direct the operation of an array of DMA engines that link the very high-speed off-chip I/O with each memory bank. In this way, the embedded processors would orchestrate the DSP pipeline operation, pulling data in before it is needed and pushing data out when it has been finished with.

The library of FPGA-optimized DSP algorithms would be stored as FPGA bit images in an off-chip flash memory device. The library would consist of all the typical DSP-orientated functions (FFTs, FIRs, convolutions/correlations, etc.) and a number of the more specialized functions (QR decomposition, Cholesky decomposition, etc.). A variety of cores for each function could be provided to enable the full range of options. Each core is also likely to provide a certain amount of configurability to reduce the total number of cores required. These cores could be loaded into the IP sockets using partial reconfiguration techniques under the control of the PowerPC socket manager.

It would also be possible for bespoke functions to be pre-implemented and included in the library. These functions may have been modeled in the Matlab or C environment and then ported into the FPGA domain using specialized tools that are being developed by the FPGA vendors.

Thus, the FPGA reconfigurable DSP pipeline would be reconfigurable at three levels:

- IP support infrastructures – choose from a variety of preconfigured options
- IP sockets – choose from a library of optimized FPGA implementations
- IP configuration – each IP block can be configured within certain constraints

Each of these can be changed dynamically by the user PowerPC CPU.

The user PowerPC CPU would remain a fixed feature of the FPGA reconfigurable DSP pipeline. Code can be developed and debugged using industry standard tools and the processor is capable of running an RTOS (e.g., VxWorks). The board can be run as a stand-alone DSP node, or it can be incorporated into

The FPGA reconfigurable DSP pipeline represents one possible way of making the power of FPGA technology available to a DSP engineer who is unfamiliar with working in the FPGA development world.

a higher-level DSP system management tool suite, such as Radstone's AXIS Advanced Multiprocessor Integrated Software development facility. The sidebar "Pipelined DSP Implementation Using FPGAs" illustrates how the FPGA reconfigurable DSP pipeline could be used to maximize system throughput in a typical DSP-oriented scenario.

Additional Advantages

Being able to implement more of the various functions within a single device has a number of other advantages that should be considered. These advantages are mainly due to the reduced transportation of data between functional nodes. Figure 2 shows a typical DSP system made up from FPGA devices and DSP processors. The time taken for data to propagate through the system is made up of processing time (Tproc) and time taken to move data from one node to another (Tmove). Although these two operations can be performed at the same time, for a system that has double buffered frame storage at each node, the overall latency is calculated by adding all these frame times together.

Using the pipelined FPGA system described in this article, all the transportation times (Tmove) are removed from the calculation because the data stays in the same memory devices and the FPGA is reconfigured to be able to perform the next required function. The system latency is reduced by a factor of approaching 50% for large systems.

As well as reduced latency, this approach consumes less of the available backplane bandwidth and requires less actual hardware to perform the same functions. This means reduced cost, power and space requirements, which could be used for additional functionality in the system. It should also be noted that Tproc3 in the FPGA implementation is likely to be less than Tproc3 in the processor implementation.

Reconfigurable Implementations

The FPGA reconfigurable DSP pipeline represents one possible way of making the power of FPGA technology available to a DSP engineer who is unfamiliar with working in the FPGA development world. Some exciting new technologies, including FPGA partial reconfiguration, multi-port DMA engines and algorithm to RTL toolsets, are pulled together by the proposed approach to provide the DSP engineer with a hugely powerful and flexible DSP Engine.

Beyond providing FPGA DSP capability to a developer unfamiliar with FPGA fundamentals, the approach also allows reconfiguration so that the pipeline can be optimized for various applications: this can be changed dynamically by the software to be a different pipeline as and when appropriate. Another key benefit of this approach is the ability to stream data in and out of the FPGA without impacting the raw performance of the embedded algorithms. ▮▮

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FPGAs Boost Processing Capabilities of Complex Signal Environments

Commercial hardware featuring multi-channel A/D converters with scalable FPGA-based processing systems permit the design and fielding of demanding real-time signal processing systems, while adhering to strict SWAP constraints.

Craig Petrie, Product Manager
George Carr, Senior Systems Engineer, Nallatech

Increasingly, complex modern signal environments are placing greater demands on signal processing systems employed across a variety of Command, Control, Communications, Computers, Intelligence, Surveillance and Reconnaissance (C4ISR) applications. The challenges of reducing the size, weight and power (SWAP) properties of new sensor systems, while also improving bandwidth, signal fidelity and efficiencies in spectrum usage, are forcing military system designers to reassess selection of system architectures and technology.

The use of complex sensors and processing of the data produced are key elements of successful embedded defense systems such as radar and software defined radio (SDR). The clear aim of complex sensor systems is to sense faster, more accurately, over a wider range of conditions and with guaranteed levels of

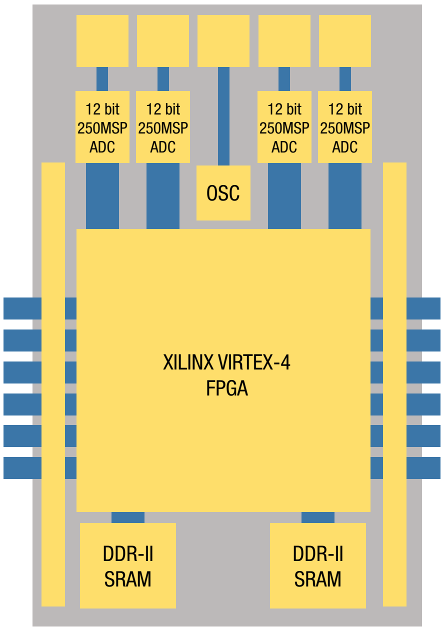
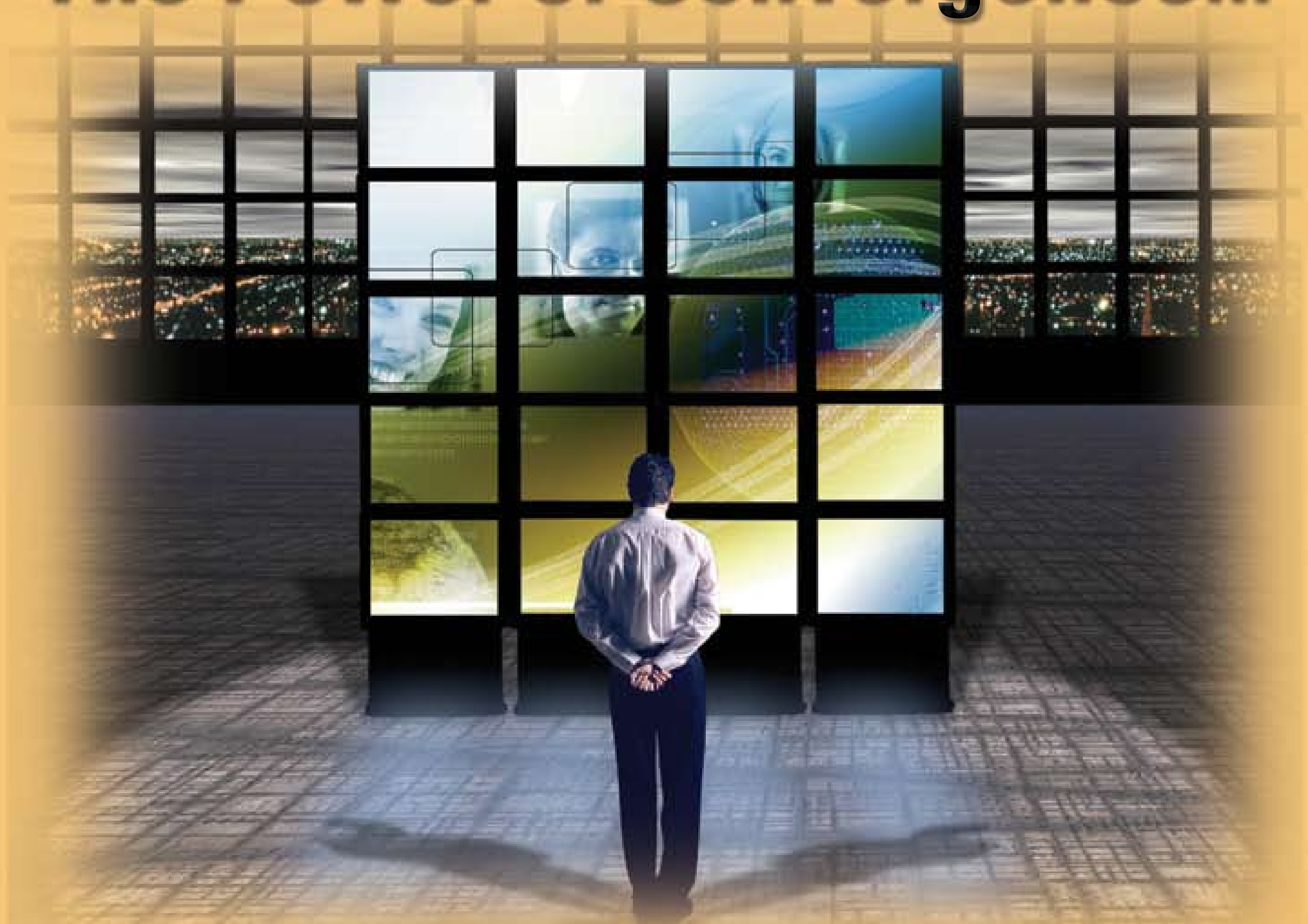


Figure 1

Quad A/D converter Xilinx Virtex-4 FPGA module.



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		Pentium® M				Intel® Celeron®						AMD Geode			486DX	
Bus	AT Expansion Bus			✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
Bus	PCI Universal Expansion Bus	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓		✓	✓		
Bus	PCI Bus Masters	4	4	4	4	4	4	4	4	4	4		4	4		
Bus	APIC (add'l PCI interrupts)	9	9	9	9	9	9	9	9	9	9					
CPU and BIOS	CPU Max Clock Rate (MHz)	1400	1400	1400	1400	650	650	650	650	650	650	333	333	333	100	100
CPU and BIOS	L2 Cache	2MB	2MB	2MB	2MB	256k	256k	256k	256k	256k	256k	16K	16k	16k	16k	16k
CPU and BIOS	Intel SpeedStep Technology	✓	✓	✓	✓											
CPU and BIOS	ACPI Power Mgmt	2.0	2.0	2.0	2.0	1.0	1.0	1.0	1.0	1.0	1.0					
CPU and BIOS	Max Onboard DRAM (MB)	512	512	512	512	512	512	512	512	512	512	256	256	256	32	32
CPU and BIOS	RTD Enhanced Flash BIOS	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
CPU and BIOS	Nonvolatile Configuration	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
CPU and BIOS	Quick Boot Option Installed	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
CPU and BIOS	USB Boot	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓					
Peripherals	Watchdog Timer & RTC	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
Peripherals	IDE and Floppy Controllers	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓		✓
Peripherals	SSD Socket, 32 DIP						1		1		1	1	1		2	1
Peripherals	ATA/IDE Disk Socket, 32 DIP	1	1	1	1	1		1		1				1		
Peripherals	Audio	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓					
Peripherals	Digital Video	LVDS	LVDS	LVDS	LVDS			TTL	TTL	LVDS	LVDS	TTL	TTL	TTL		
Peripherals	Analog Video	SVGA	SVGA	SVGA	SVGA	SVGA	SVGA	SVGA	SVGA	SVGA	SVGA	SVGA	SVGA	SVGA		
Peripherals	AT Keyboard/Utility Port	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
Peripherals	PS/2 Mouse	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓		
Peripherals	USB Mouse/Keyboard	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓		
I/O	RS-232/422/485 Ports	2	2	2	2	2	2	2	2	2	2	2	2	2	2	2
I/O	USB 2.0 Ports	2	4	2	4											
I/O	USB Ports					2	2	2	2	2	2	2	2	2		
I/O	10/100Base-T Ethernet	1		1		1	1	1	1	1	1	1	1	1		
I/O	ECP Parallel Port	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
I/O	aDIO(Advanced Digital I/O)	18	18	18	18	18	18	18	18	18	18	18	18	18		
I/O	multiPort(aDIO, ECP, FDC)	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓		
SW	ROM-DOS Installed	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
SW	DOS, Windows, Linux	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓

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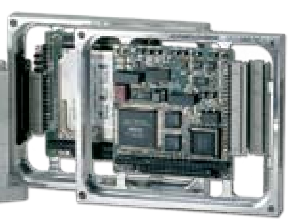

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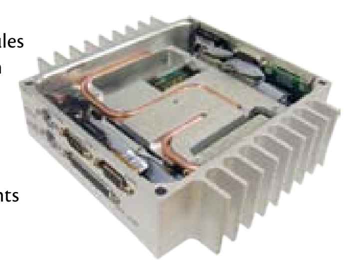

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Bus	AT Expansion Bus	✓		✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
	PCI Expansion Bus Master	✓	✓				✓							✓	✓
	McBSP Serial Ports	✓	✓				✓								
Analog Input	Single-Ended Inputs	16	16	16	16	16	16								
	Differential Inputs	8	8		8	8	8								
	Max Throughput (kHz)	1250	1250	40	500	100	1250								
	Max Resolution (bits)	12	12	12	12	16	12								
	Input Ranges/Gains	3/7	3/7	3/1	3/4	1/4	3/6								
	Autonomous SmartCal	✓	✓												
	Data Marker Inputs	3	3		3		3								
Conversions	Channel-Gain Table	8k	8k		8k	8k	8k								
	Scan/Burst/Multi-Burst	✓	✓		✓	✓	✓								
	A/D FIFO Buffer	8k	8k		8k	8k	8k								
	Sample Counter	✓	✓		✓	✓	✓								
	DMA or PCI Bus Master	✓	✓		✓	✓	✓	✓						✓	
	SyncBus	✓	✓				✓								
Digital I/O	Total Digital I/O	16	16	16	16	16	16	16	48	18/9	32	64	32	48	48
	Bit Programmable I/O	8	8		8	8	8	8	24	6/0				48	✓‡
	Advanced Interrupts	2	2		2	2	2	2	2					2	
	Input FIFO Buffer	8k	8k		8k	8k	8k							4M	8M
	Opto-Isolated Inputs										16	48	16		
	Opto-Isolated Outputs										16	16			
	User Timer/Counters	3	3	3	2	3	3	3	3	3				10	6
	External Trigger	✓	✓		✓	✓	✓	✓	✓					✓	
	Incr. Encoder/PWM									3/9					✓‡
	Relay Outputs												16		
Analog Out	Analog Outputs	2	2		2	2	2	4							
	Max Throughput (kHz)	200	200		200	100	200	200							
	Resolution (bits)	12	12		12	16	12	12							
	Output Ranges	4	4		3	1	4	4							
	D/A FIFO Buffer	8k	8k				8k	8k							

‡ User-defined, realizable in FPGA

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reliability. Such requirements force system designers to incorporate a variety of complex sensors in greater numbers.

Until relatively recently, the first stages of radar signal processing systems were performed in the analog domain. The trend has been to move the A/D converter closer to the radar antenna in the signal processing chain and perform more processing in the digital domain. Digital hardware offers robust system stability, flexibility in waveform and filter design, the ability to develop adaptive processing algorithms and an effective upgrade path.

As front-end radar signal processing functions move into the digital domain, the signal processing requirements of the digital hardware increase dramatically. This increase is driven by the direct sampling of analog data streams at rates well into the GHz range. The increased sampling rates and increasingly complex signal environments force more complex front-end algorithms, such as digital up/down conversion and filters, which further drive computational requirements of the digital processing engines. FPGA-based systems are well suited to meet the SWAP and environmental constraints as signal processing systems are fielded on rugged platforms ranging from armored vehicles to UAVs.

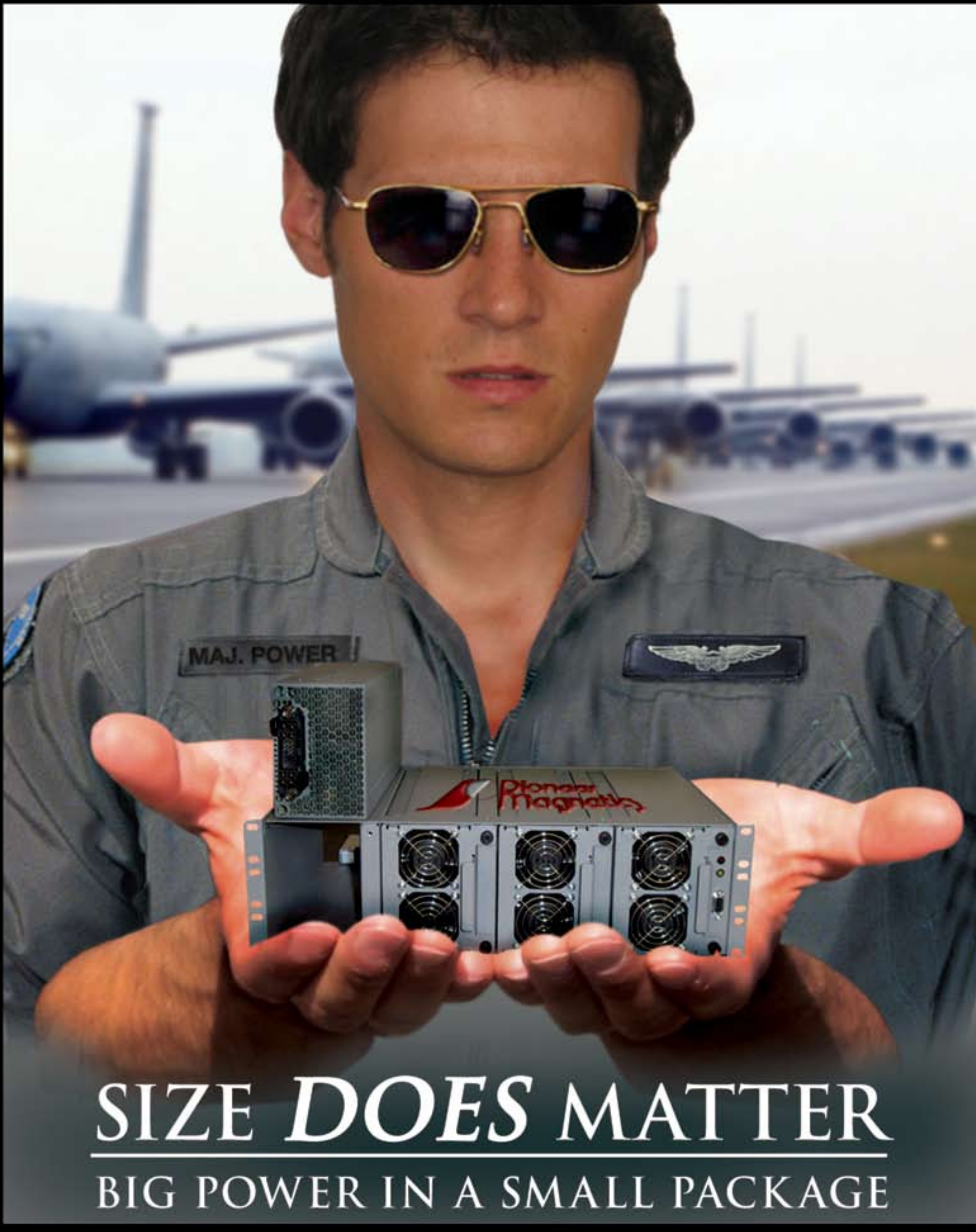
FPGA-Based Digital Signal Processing

The general complexity of input signals and increased data rates result in a substantially greater processing requirement that exhausts the capability of traditional processing technologies such as DSPs. Such limitations have been well documented in recent years, with alternative technologies and signal processing techniques proposed to alleviate the processing bottleneck. During this time, FPGAs have rapidly gained acceptance in military defense applications as a preferred processing technology. They are well suited for very high-speed parallel multiply and accumulate functions and are therefore an ideal processing device for DSP operations such as Fast Fourier Transforms (FFTs), Finite Impulse Response (FIR) filters, digital down-converters (DDCs), digital up-converters (DUCs), correlators and pulse compression.

The transition of FPGAs from a "disruptive technology" to the technology of choice for many new military programs has reshaped the competitive landscape of commercial hardware and software solutions used in military applications. An ecosystem of new companies offering FPGA solutions and professional design services has flourished, while established players with product portfolios built around RISC processor technologies have evolved their product offering to include both DSPs and FPGAs.

Building Compact Sensor Processing Systems Using FPGAs

The Xilinx Virtex-4 family of FPGAs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boasts computational density and high-throughput capabilities that allow the placement of the processing engine to be integrated with the A/D converter front-end. This permits immediate processing of the digital data with a number of significant advantages. These include processing raw sensor data in real time, the ability to operate DSP algorithms at appropriate arithmetic word lengths, superior SWAP properties compared to RISC processors, the ability to scale the number of input channels with relative ease and the ability to distribute complex DSP algorithms over multiple FPGAs.

The power and density savings of FPGA-based digitization and processing systems allow military design engineers to build embedded systems with one to four FPGA cards that would typically require hundreds of DSP or PowerPC/Altivec processors partitioned across multiple racks. Distributing the digital data from an A/D converter to hundreds of PPCs in a VME system can be the bottleneck to building a complicated processing system. The reduction in the number of processing devices achievable using FPGAs and the use of multi-gigabit connections help solve the data distribution issue.

A DSP-based radar processing system built with the goal of capturing and processing a 100 MHz bandwidth may need a sampling rate of 250 MHz with a 12-bit sample. Transmitting the sample data in chunks to a farm of 100 PPC processors can max out even a robust interconnection network. Often, this sample data becomes 8 bytes as it is processed in an FFT or other transform. Feeding the transform output to other downstream processing devices can be tougher than getting the sample data to the hundreds of processors to begin with. The resultant product out the back-end can be several orders of magnitude less than the digital data rate coming in, but the processing system must be built to handle multiple gigabyte/s networks required by the number of discrete processors in the system.

An equivalent radar processing system built using commercial FPGA hardware and IP cores from Nallatech illustrates the benefits of sensor processing systems featuring multiple A/D converters with attached scalable FPGA-based architectures.

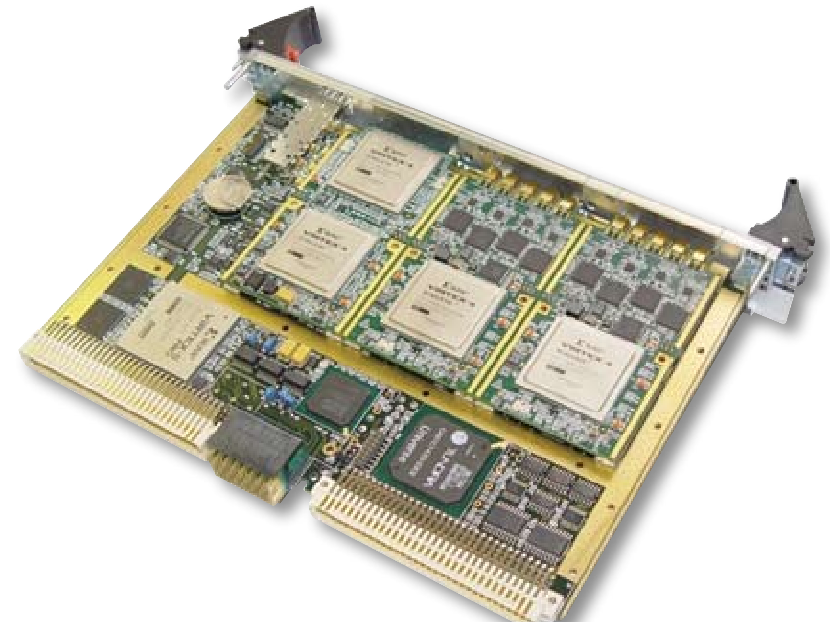

Figure 2

VITA-41 carrier card supporting eight A/D converter channels directly coupled to four Xilinx Virtex-4 FPGAs.

The Nallatech BenADC DIME-II module featuring four A/D converters directly coupled to a Virtex-4 FPGA can digitize four analog inputs at the rate of 250 Msamples/s at 12 bits (Figure 1). The onboard Virtex-4 FPGA handles much of the front-end data processing that would have been dealt with by multiple PPCs in the previous configuration. A Virtex-4 LX160 FPGA implementing floating-point FFTs can process sensor data at a rate of approximately 40 GFLOPs/s while consuming only 15W.

A/D converters can be added to the system to accommodate additional input channels by populating another BenADC module onto the VITA-41 DIME-II carrier card (Figure 2). This example configuration illustrates the use of eight A/D converter inputs and external clock inputs directly coupled to each of the Virtex-4 BenADC FPGAs. The VITA-41 carrier card supports three module sites, providing the system designer with the luxury of additional FPGA processing resources or memory depending on the complexity of the signal environment. The result is a much simpler architecture requiring orders of magnitude less power, cooling, weight and cost.

The latest generations of commercial hardware featuring multiple A/D converters with scalable FPGA-based processing systems permit the design and fielding of compact systems to handle both the increased data load and processing requirements of today's complex sensor processing systems. Front-end processing using FPGAs tightly coupled to multiple A/D converter channels can dramatically reduce the amount of data that must be transmitted across a system. Complex real-time processing applications such as radar, SDR and signal characterization can be processed within the FPGA fabric at close proximity to the sensor, resulting in a significant simplification of system architecture while improving overall performance.

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Eldersburg, MD.
(877) 446-2552.
[www.nallatech.com].

Selecting Architectures for Signal Processing in Military Applications

When it comes to signal processing, choosing the appropriate application partitioning as well as the right combination of devices depends on both technology and economical criteria.

Ram Sathappan, Software Defined Radio Business Manager, Leon Adams, Catalog DSP Marketing Manager, Texas Instruments

Real-time signal processing is a driving element in the evolution of many military applications, such as software defined radios, weapons navigation systems and early warning radar systems.

Each of these applications works with a signal or stream of data. Processing these signals in the digital domain offers significant advantages over working with analog signals. Digital signals maintain their integrity over longer distances than analog signals and can also be precisely reproduced without degradation. Additionally, working with signals in the digital domain simplifies enhanced signal processing, adjustment of resolution or bit rate and movement between different codec formats to increase device interoperability. Execution of effects, such as audio echo cancellation and noise reduction algorithms, is also facilitated by digitally processing signals.

Signal filtering and cleanup is also simplified when working with digital, as filtering analog signals requires closely matched and expensive components whereas digital filtering is implemented in flexible code. Furthermore, improving digital signal quality or channel density is a matter of increasing the performance of the processor, and programmable processors, such as DSPs, enable developers to continually improve quality without redesigning hardware.

Developers have a variety of architectures to choose from when developing digital signal processing applications. Embedded systems generally use four different types of advance processing devices to execute digital signal processing: ASICs, FPGAs, general-purpose processors (GPPs) and DSPs. When selecting architectures for military applications, developers must balance cost, power, perfor-

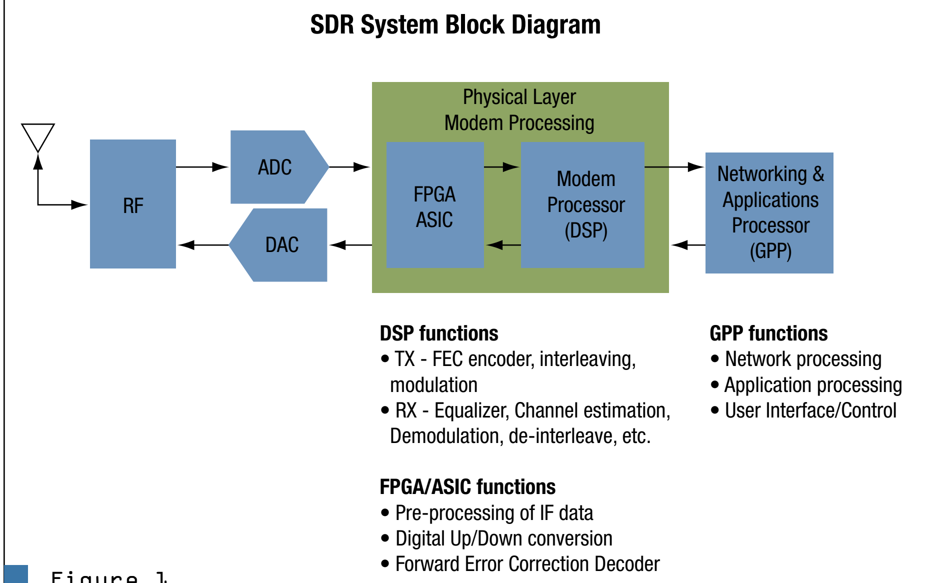

Figure 1

An example SDR system block diagram implements multiple architectures, including ASIC, FPGA, general-purpose processor (GPP) and DSP.

Decision Table for Designers of Real-Time Applications

	Time to Market	Performance	Price	Development Ease	Power	Feature Flexibility	Summary
ASIC	Poor	Excellent	Excellent	Fair	Good	Poor	Fair
DSP	Excellent	Excellent	Good	Excellent	Excellent	Excellent	Excellent
FPGA	Good	Excellent	Poor	Excellent	Poor	Good	Fair
GPP	Good	Good	Fair	Good	Fair	Excellent	Good

Table 1

The criteria used to evaluate these different architectures in real-time applications such as signal processing are listed across the top, according to the importance of the criteria and the effectiveness of individual choices in meeting those criteria.

mance, flexibility and reliability to meet the demands of their mission-critical operations. For each architecture, there is a different set of tradeoffs (Table 1).

Picking the Right Foundation Architecture

With ASICs, like FPGAs, developers can tune all the different parameters of the processor to meet the needs of the design, offering high application-specific performance. ASICs can achieve decent power efficiency when the design is targeted for low power. Also, standard cell logic gates with no overkill or underkill are the most efficient and smallest semiconductor chip size, thus likely to offer a low recurring price. ASIC commoditization can also drive down the price per gate of ASIC chips.

It is important to note that, by their nature, these devices take a unique approach to a target application so they are very limited in flexibility. The development cycle is long and expensive, typically running more than $1 million in non-reoccurring engineering (NRE) charges. If any design parameters change in the development cycle, the entire ASIC must be respun, a process that can consume additional months and significant additional NRE costs.

FPGAs can be optimized for specific applications and provide powerful performance without the delays and costs associated with respinning an ASIC. FPGAs also offer more flexibility than ASICs and can be field-reconfigured for additional features or changes. Developers should consider the fact that hardware reprogramming of an FPGA can be significantly more difficult than software programmable solutions. FPGA devices come with a price premium, which is a factor when developing high-volume applications. Due to FPGA circuit technology, as well as the overhead power of unused gates in the array, FPGAs are not very power efficient.

GPPs offer programmability and therefore flexibility, allowing faster development cycles for the desired function versus ASICs. With proper use of high-level programming and/or use of standard code modules, development time can be cut significantly, thus saving in development cost.

GPPs are often not oriented toward embedded applications, focusing instead on general computer purposes such as database management and protocol processing. They typically are not efficient in multiply/accumulate-intensive digital signal processing applications. In order to keep silicon costs down for these applications, GPPs typically offer a moderately efficient multiplication instruction that takes several cycles to complete. In addition, adding the result of each multiplication requires another instruction. This ultimately limits the performance and power efficiency of the GPP.

DSPs are optimized for signal processing applications and offer many architectural features that reduce the number of instructions necessary for efficient signal processing. In other words, comparing performance is much more than counting instructions. What really needs to be measured is how much work is actually done. For example, the VLIW architecture of TI's TMS320C64x generation of DSPs can initiate up to eight operations per clock cycle and execute up to eight 16-bit multiply/accumulates per cycle.

Integrated specialized compute engines increase performance by executing complex functions in hardware. DSPs are also optimized for specific applications by providing a balanced mix of performance, integrated peripherals and on-chip memory. The programmable flexibility of DSPs enables developers to implement complex algorithms in software. Not only can a DSP support a video codec like MPEG-2 and easily handle different resolutions with a simple software upgrade, it can implement emerging codecs and standards as they arise without a hardware redesign. The same DSP can also include software defined radio (SDR) modem processing.

Combining Architectures to Actualize Complex Designs

As systems become increasingly complex, developers are turning to multiple architectures to meet their design needs. For example, the Joint Tactical Radio System (JTRS) program for developing next-generation military communication devices envisions the use of SDR technology with standardized hardware to support a varied range of voice, data and wideband networking waveforms, or protocols, used in military radios.

To achieve a balance between reduced costs, lower power consumption and the support of multiple waveforms, the right combination of GPPs, DSPs, ASICs and FPGAs is needed for baseband, networking and application processing. For example, an SDR system block can implement multiple architectures (Figure 1).

For the processing of the physical layer in SDR systems, a combination of high-performance logic and digital signal processing is needed to support the different methods of digital up/down-conversion, modulation and demodulation. Digital up/down-conversion can be processed using ASICs in the case of single-protocol radios for best-in-class cost and power, but in SDR systems supporting multiple waveforms, this requires flexible logic and thus involves the use of FPGAs. The dynamic real-time processing of the DSP then takes over from the FGPA in implementing modulation and demodulation of the signal.

The system of error control for data transmission in wireless modems, called forward error correction, can be implemented in either DSP or hardware gates, depending on the type of encoding/decoding algorithms used. For example, Reed-Solomon encoding and decoding algorithms, along with encoding for convolutional and turbo codes, can be programmable and is better implemented on DSPs for best cost/power benefits. The more complex, cycle-intensive techniques, such as decoding convolutional or turbo algorithms, are best implemented using hardware gates, such as an ASIC or an FPGA.

The media access control (MAC) layer for network processing involves encoding and decoding packets into bits and transmission to and from the network interface as well as flow and conflict management of data packets within a channel. This networking processing requires an RTOS and involves a lot of control functions. The best processing element to implement MAC functions, as well as the memory management needed in RTOS, requires GPPs or microprocessors/controllers.

Thus an optimal combination of GPP, DSP, ASIC and FPGA components defined by the critical parameters of power, performance and cost are a necessity in real-time signal processing systems for military applications such as software radios. ❚❚

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FPGAs and DSPs Make a Complete Signal Processing Solution

The best solution for military signal processing applications is a hybrid architecture that takes advantage of the strengths of both FPGAs and DSPs.

Jeffry Milrod, President and CEO
BittWare

In technical publications over the past year, the question of whether FPGAs will replace DSPs in various applications, including signal processing, has been posed ad nauseam. Although this may be an interesting topic of discussion, the truth remains that DSPs and FPGAs are, in fact, very different technologies with different strengths and weaknesses. FPGAs can be very good at solving well-defined, high-speed, repetitive problems. DSPs are better at implementing highly complex algorithms as well as applications that involve some sort of decision-making, adaptive processing or algorithms that may change frequently.

Real-world, embedded military signal processing applications often require both of these types of processing and would benefit from having access to both technologies. Therefore, the optimal solution for a general-purpose signal processing board should include both FPGAs and DSPs, thus creating the need for developing hybrid signal processing architectures that leverage the strengths of both.

Issues to Overcome in Hybrid Architectures

Although hybrid architectures are simple in concept, i.e., integrating DSPs and FPGAs onto one board, significant issues must be addressed for the final architecture to be effective. The crux of the problem is how to best handle data flow both between the FPGA and DSP compute elements, and to and from the hybrid architecture through real-world data interfaces. Another noteworthy complication is how to best enable the host access to the compute elements for command and control.

One of the biggest challenges faced when designing a hybrid architecture, i.e., the one that most directly impacts signal processing performance, is how to handle the communication between the FPGA and DSP compute elements. Of course, these interfaces must be tightly coupled, have low latency and be deterministic.

Less obvious is the fact that, in most scenarios, the communication speed between the DSP and the FPGA must be significantly faster than the board's I/O bandwidth since it is possible that the data will need to move from DSP to FPGA several times before signal processing is complete.

On BittWare's GT-3U-cPCI Hybrid Signal Processing board (GT3U), all data enters the board through the FPGA I/O interface (Figure 1). Once the data has entered the FPGA, the option exists to provide pre-processing before sending it along to the DSP(s) via dedicated communication link ports.

At this point, depending on the pre-processing algorithm being used, the data rate may decrease, remain the same or increase slightly. The transfer rate between the FPGA and DSP(s) must, then, at minimum, equal the I/O data rate. More optimally, that transfer rate must be many times faster that of the I/O. Each link port provides 500 Mbytes/s bi-directionally for a total of 8 Gbytes/s of data transfer between the DSPs and the FPGA.

Given the advantages of using the FPGA for straightforward, repetitive processing, it makes sense to have all onboard I/O enter through the FPGA. In addition to providing powerful front-end processing, system designers also gain the ability to support a wide variety of data transfer mechanisms and protocols. Many newer board formats that support high-speed serial interfaces (SerDes) can benefit greatly from this architecture, since the FPGA can implement several different protocols. The I/O flexibility provided by the FPGA has become increasingly important as the days of one or two dominant I/O standards has faded.

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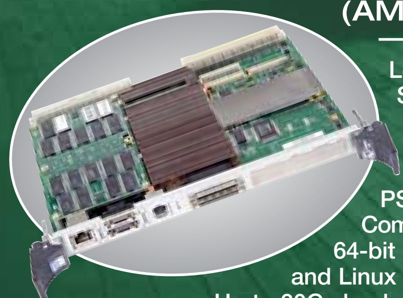

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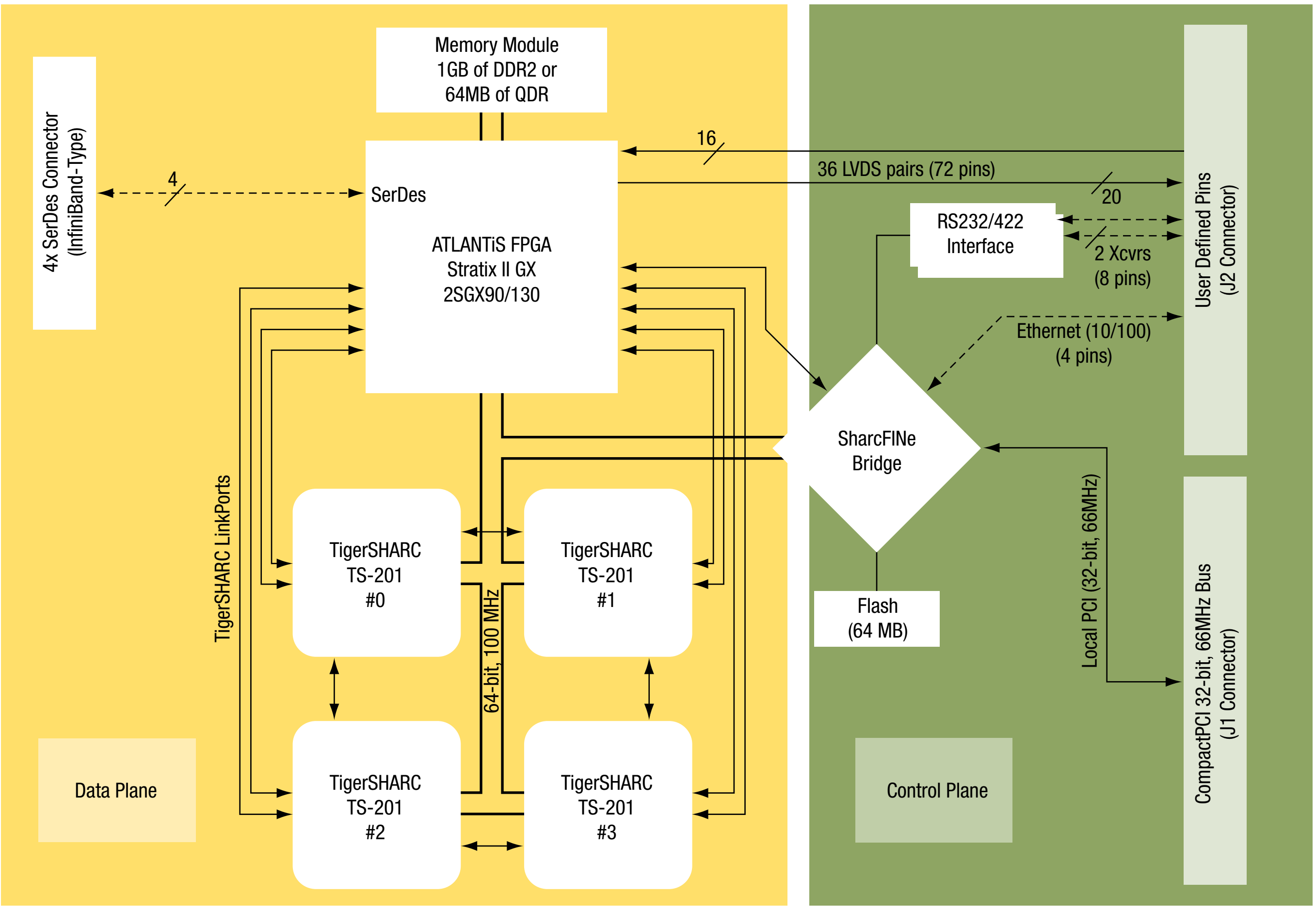

Figure 1

Hybrid signal processing block diagram details communication paths between the FPGA and DSPs.

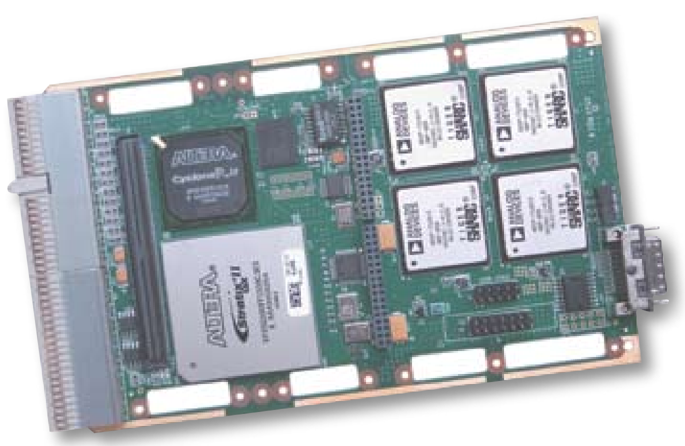

Figure 2

A ruggedized 3U CompactPCI hybrid signal processing board, designed for demanding multiprocessor-based applications requiring complete flexibility and adaptability, combines both a high-density FPGA and a DSP processing cluster.

Another challenge for a hybrid architecture is how to seamlessly integrate the diverse compute elements into a system. This is primarily a requirement for host interface and control mechanisms that connect the hybrid compute resources to standard host interfaces. In most systems today, this is done via PCI and/or Ethernet.

An optimal solution is to route all host communication through a separate control plane, orthogonal to the data flow. In the GT3U, this is handled by the SharcFINe host bridge, implemented in an Altera Cyclone II. This bridge connects the PCI bus to an onboard command and control bus that extends to each onboard FPGA and DSP. Since the control bus is independent of the data link ports, it allows the host to directly access and control each onboard compute resource without impacting data flow.

Using a Hybrid Architecture

Although the DSPs might do much of the heavy lifting in regard to signal processing, the FPGA is responsible for handling all transfer of data on and off the board, and between itself and the DSP(s), while also providing user-defined pre-, co- or post-processing. Developing the application processing IP is challenging. Integrating it into an FPGA in a hybrid architecture with fixed pinouts and external interfaces is even harder.

An FPGA framework that can facilitate this is required, one that also supports software-controlled data routing between all modules within the FPGA and enables the user to easily insert processing modules at any point in the data flow. With an FPGA framework such as this in place, the command and control bus can configure the data flows for a given application among the I/O interfaces, IP processing modules and DSP(s).

The ATLANTiS architecture, implemented in each onboard FPGA on the GT3U, provides such a framework, thus enabling the DSP(s) to communicate with all other I/Os connected to the board in a point-to-point, multicast or broadcast fashion. The I/Os can be connected or disconnected from each other as requirements dictate without the need for recompiling or changing cables.

This architecture consists of all of the hardware interface modules along with one or more data switches that are connected to a configuration register controlled by the user via control software running on the DSPs or the host. The routing can be changed at any point by reprogramming the configuration registers. Since all I/Os connected to the board are input into the FPGA, and thus into the framework itself, standard and/or custom FPGA processing blocks can be easily inserted into the data flow at any point.

The Future in Hybrid Design

The brute force method of adding either more DSPs or more FPGAs to a single board slot has not only failed to keep up with the demands of real-world applications, but also limits military system designers to the strengths and weaknesses of a single technology. Signal processing vendors should be focused on providing their customers with hybrid signal processing boards that are architected to mitigate the weaknesses and risks of each technology. The GT3U (Figure 2) utilizes a hybrid signal processing architecture that features a high-gate count Altera Stratix II FPGA and four ADSP-TS201S TigerSHARC processors from Analog Devices, giving system designers the best of both worlds. ▮▮

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Case Study: Portable RF Test System Exploits PXI

An integrated portable RF field test system leverages PXI and high-speed data recording technology, resulting in an ideal test solution for military radios.

Lance Butler, Senior Systems Integrator
National Technical Systems
Phil Brunelle, Co-Founder and V.P. of Engineering
Conduant

Many designers face the same problem when developing Radio Frequency (RF) receiving devices such as satellite radios, cell phones and other wireless products. They need to test their prototypes in real-world environments although there are several difficulties involved in bringing their products to the field for testing. Rigorous testing will lead to improvements in software/firmware algorithms, better chipset design and overall availability levels. The RF satellite application discussed in this case study is aimed at general RF applications, but it is an ideal platform for testing military radios and other communications devices that work within the RF spectrum.

A major difficulty in testing RF devices is that the environment is constantly changing due to seasonal factors such as wind, rain or snow or even foliage on trees. The environment also changes with the construction of buildings and installation of new broadcast sources. One must also account for performance while the device is moving in an automobile or other mode of transportation. These factors can lead to many visits to the field. In addition, imagine trying to test for snow effects in July or dry summer heat in December. Another important consideration are the logistics involved with bringing large quantities of product into the field for test-

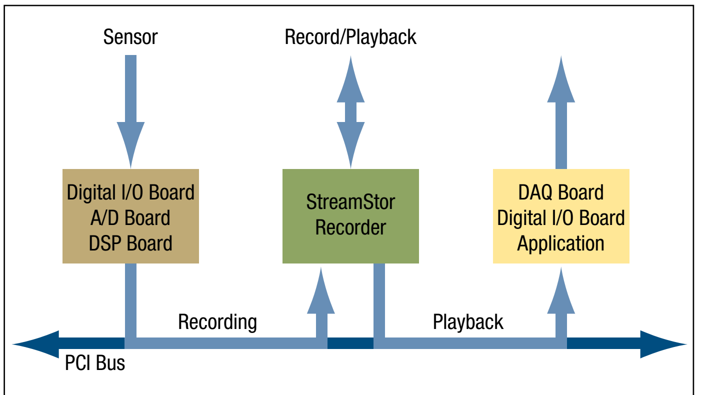

Figure 1

Conduant's StreamStor Recorder in a typical record/playback system implementation.

Figure 2

Portable version of a PXI combination record and playback system with GPS.

ing. Particularly in a production environment, the thought of testing product in the field is daunting considering the manpower alone.

Integration to the Rescue

A recently designed system solves all of these problems by replaying real-world environments in the lab or on the production floor. Test personnel can now travel to any given location just once and quickly record the RF environment, and then playback and manipulate that signal set in the lab under controlled conditions to an unlimited number of units under test (UUTs).

For example, a company testing satellite radios might record a set of files in a metropolitan area periodically through the year to capture effects of various seasons, weather effects and topology. They might also record under difficult circumstances in open areas. These files can then be reliably played back repeatedly in the lab so that different designs can be tested with the same signal set in order to compare the strengths and weaknesses of those designs.

The open architecture of the PXI platform (an electronic instrumentation platform) is the key to making this system a reality. The system is comprised of National Instrument devices that take advantage of their strength in RF and modular design married together with Conduant hardware that makes use of their specialization in extremely fast data recording and playback. PXI allowed engineers at systems integration firm NTS to marry those technologies and create a solution

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With PXI, users benefit from the low cost, ease-of use, modularity and flexibility of PC technology. Use of this standard allowed NTS to build and deliver the system described here on a very tight one-month schedule.

that was portable and offered high-speed field recording and in-lab playback.

How it Works

Field RF input signals are routed through a RF Preamp, when needed, to increase the signal levels so that they are suitable for recording. The signal is then run through a 2.7 GHz RF Vector Signal Analyzer for down-conversion to an appropriate frequency. A 14-bit Digitizer then progresses the IF signal and routes the digital data through a DMA channel. A Conduant StreamStor card then funnels the data onto a Conduant Big River DM 4 Recording chassis at 100 Mbytes/s. If needed, data recording rates of 400 Mbytes/s are possible. The recording system provides 1.6 terabytes of storage capacity. The diagram in Figure 1 shows how StreamStor works in a system.

This combination allows massive amounts of data to be recorded for over 4 hours without interruption. While additional drive arrays are available for additional recording time, this duration was found to be sufficient for this application. For the playback process in the lab, signals are essentially routed in the reverse order through playback hardware. The StreamStor card feeds data from the drives to the DMA channel to a 2.7 GHz Vector Signal Generator with Digital Up-conversion. The data is then played through a digital to analog converter (DAC) and restored to the recorded frequency, and sent to the devices being tested.

A utility is provided to further extend the capabilities of this system by allowing files to be moved to or from the drives. In the former case this allows files to be ported into any analysis package, such as Diadem or Matlab, where they can be

analyzed or modified. The latter case allows for synthesized signals to be played in order to simulate various effects. As an example, a user may record a given signal and then modify it to simulate periodic signal strength loss. This new file can then be played in order to test the effects of the change versus the original file.

Flexible PXI Allows for Many Options

The most common configurations involve a recording system in a portable package that typically includes a shock-resistant shippable container for the field and a rackmount playback system for the lab. However, thanks to the modular nature of PXI and the power of LabVIEW software from NI, other configurations have been developed for various needs. PCI eXtensions for Instrumentation (PXI) is the open, multi-vendor standard for measurement and automation that delivers more than 10 times the performance of older measurement and automation architectures. With PXI, users benefit from the low cost, ease-of use, modularity and flexibility of PC technology. Use of this standard allowed NTS to build and deliver the system described here on a very tight one-month schedule.

An example of this flexibility allows for quick reconfiguration. When a source signal is readily available at the lab, but the requirement for testing multiple UUTs with the same signal exists, the two systems can be combined in one chassis. This version uses an 18-slot PXI chassis to house components of both the record and playback system and uses the same LabVIEW software as the other systems.

If two channels need to be synchronously recorded, additional hardware can be added. In this case the RTSI (Real Time System Integration) bus inherent in PXI allows very tight synchronization of the two channels. The two channels can come from different sources for diversity testing, or they can be set for different frequencies. The two-channel playback version of this system maintains the synchronicity throughout the process. PXI also allows for the integration of GPS position data into the recording. This can be useful when terrain features are of particular interest. Figure 2 shows a portable version of such a combination record and playback system with GPS.

Efficiencies of PXI Development Reduced Costs

Because the PXI standard promotes interoperability and PXI drivers are very easy to develop, this system represents a significant cost savings over other approaches. Integration of several vendor subsystems was facilitated by common interfaces and standards. Impressive field recording speeds were achieved and high quality and consistent lab playback made this project a success all around.

To support increasing bandwidth needs for the future, Conduant is embracing PCI/PXI-Express advancements and will support data recording speeds of 600 Mbytes/s. National Instruments will utilize PXI-Express to support faster digitizers and more advanced arbitrary waveform generators. ▮▮

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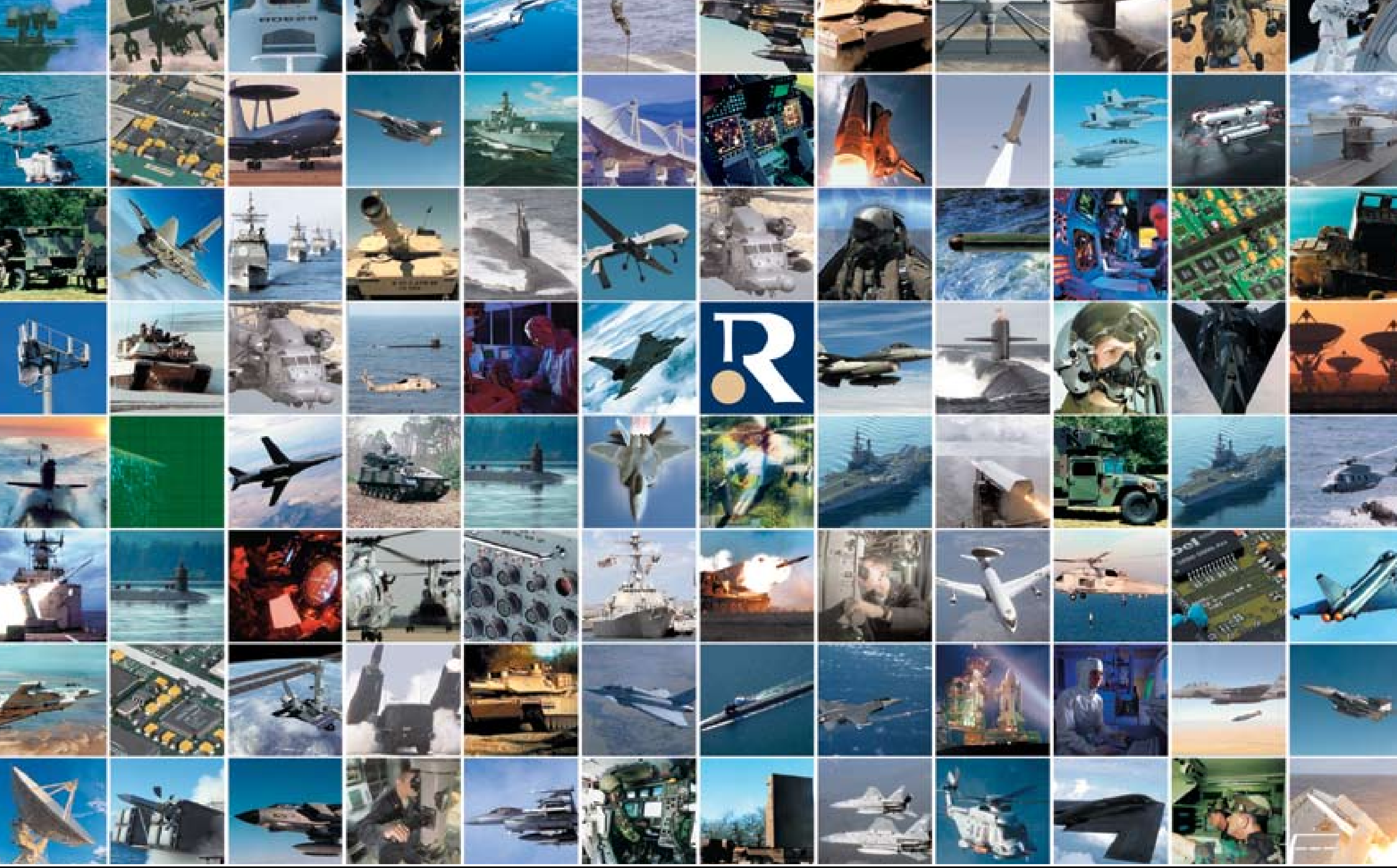

PC/104, EPIC Boards Target Small Systems

For embedded military designs in small spaces, PC/104 and its larger, younger cousin EPIC are getting attention from military system developers.

Ann R. Thryft, Senior Editor

When developers choose an SBC for military applications they have to think long-term. Not only must the technology meet the right cost and performance levels, but it must also be simple, rugged and easily maintained. Since military systems are shrinking in size, the technology must also fit into small spaces, such as military radios (Figure 1). PC/104 and its cousin EPIC meet all of those needs, and also deliver mature technology that leverages all facets of the PC.

For new designs and retrofits, chip and system architecture solutions that have already been worked out in the world of commercial desktop PCs can be leveraged with boards based on PC/104 and EPIC form-factors.

PC/104's inherently rugged design stems from its stackable, no-backplane structure, along with its pin-and-socket mating connector style. Even more ruggedization can be achieved by suppliers using a combination of design techniques, such as soldered-down memory, and thorough test and screening procedures, such as testing a board over the full temperature range.

Newer PC/104 Flavors

Other flavors of PC/104 include PC/104-Plus and PCI-104. A PC/104 card is essentially an ISA bus board reduced in size to 3.6 in. x 3.8 in. A PC/104-Plus module implements PCI on a stackable board that maintains the same form-factor. These modules can include the original PC/104 connectors for the widest range of possible system configurations.

PCI-104, a PCI-only implementation, was part of the original PC/104-Plus spec. Although PC/104's slot count is unlimited by the spec, developers typically stack no more than six cards together. In contrast, PCI-104, like PCI, allows only four cards along a bus segment. However, PCI-to-PCI bridging is a mature technology.

The most recent addition is the EPIC form-factor. This larger, younger cousin to PC/104 has won lots of fans among military system designers for its superior thermal management and size-to-performance ratio. The EPIC form-factor locates the processor out in the open away from I/O expansion boards that can be affected by its heat, and where it can be cooled more easily. Its larger board size, at 4.528 in. x 6.496 in., also allows mounting holes for a cooling arm on the CPU's sides.

In this year's crop of PC/104 and EPIC SBCs, shown in the next few pages, the amount and type of I/O continues to grow. Fast Ethernet or Gigabit Ethernet, various types of graphic support and USB are now common, reflecting the increase in networked small systems and use of displays.

Figure 1

As military systems get smaller and more mobile, PC/104 and its cousin EPIC are found in UAVs, aboard aircraft and in military radios. In Mahmahdiyah, Iraq, a radio operator for the 1st Platoon, 1st Battalion, 320th Field Artillery relays measurements for a counterfire.

Photo by: SPC Kelly K. McDowell, Courtesy of U.S. Army

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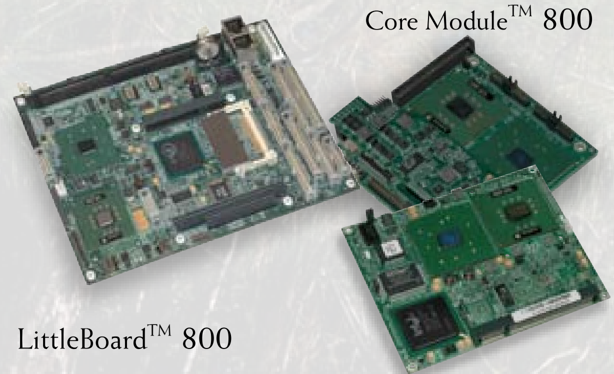

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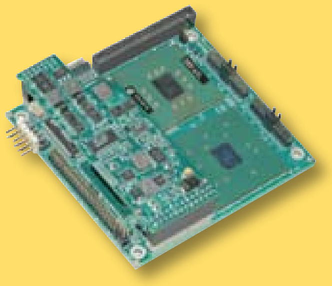
SBC Targets Rugged Mil Apps

For rugged applications that require high performance in a compact module, it's hard to beat an architecture that accommodates both. With those needs in mind, Ampro Computers offers its CoreModule800. The board is a RoHS-compliant, rugged Celeron M PCI-104 SBC that features ultra-low-power Centrino performance combined with advanced networking, high-performance graphics and all of the necessary PC-compatible component subsystems.



The board comes with either the 600 MHz or 800 MHz ULV Celeron M, 512 Kbytes (600 MHz) or 0 Kbytes (800 MHz) of L2 cache, up to 1 Gbyte of PC2700 DDR333 SODIMM, the Intel 855GME/ICH4M chipset, 400 MHz FSB and Gigabit Ethernet. PC-compatible DMA and interrupt controllers and timers, a battery-backed RTC/CMOS real-time clock, a watchdog timer, and a powerfail reset that triggers when input voltage drops below predetermined thresholds are provided.

I/O includes a single PCI-bus Enhanced Ultra DMA 33/66/100 Synchronous IDE interface that supports up to two hard drives, two RS-232/422/485 serial ports, a parallel EPP/ECP bidirectional port, USB 2.0, I/O for one or two floppy drives and a PS/2 keyboard/mouse interface. For video, the integrated Intel Extreme Graphics 2 controller is provided with an AGP 4x 128-bit 3D engine, up to 64 Mbytes of UMA frame buffer and dual-channel LVDS. The controller supports resolutions up to 2048 x 1536 and 3.3V or 5V flat panels. Volume pricing starts in the low $800s.

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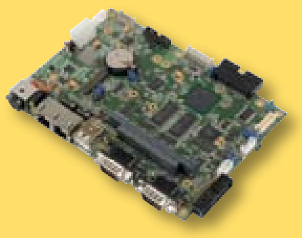
Rugged EPIC Board Consumes Only 2W Typical

For small, ultra-low-power applications, ratcheting down the amount of power consumption in a subsystem can be tough. That's why Arcom designed its ZEUS EPIC-sized SBC to consume only 2W typical. Combined with dynamically adjusted sleep modes, extensive communications options, a wide operating temperature range and a vehicle-compatible power supply, the board's ultra-low-power design makes it ideal for vehicle tracking, mobile terminals and network communications controllers.

The RoHS-compliant board is based on the Intel 520 MHz PXA270 XScale RISC processor. ZEUS has seven onboard serial ports to support a wireless modem and GPS and provides traditional hardwired serial I/O functions for legacy communications. A small adapter module fitted with a variety of GSM/GPRS, iDEN and CDMA wireless modem modules is optional. The board includes up to 256 Mbytes



of soldered SDRAM and up to 64 Mbytes of soldered AMD MirrorBit flash. 256 Kbytes of battery-backed SRAM using the onboard battery are provided.

Other features include a TFT/STN flat panel graphics controller, analog touch screen controller, dual 10/100BaseTx Ethernet ports, I^2C controller, dual USB host controller, USB client, AC97 audio/codec, CompactFlash interface, SDIO and a standard PC/104 bus expansion connector. The ZEUS may be powered from the integrated DC/DC PSU (10-30V) or from a single +5V input. The power supply has been designed for use with vehicle power looms and features transient suppression and protection. Other options include a CANbus controller and an LVDS adapter. The ZEUS is supported with ready-to-run development kits for Embedded Linux and Microsoft Windows CE 5.0. Pricing starts at $410 in quantities of $1,000.

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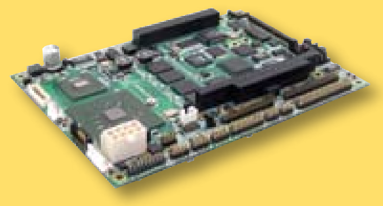
Speedy EPIC SBC Targets Data Acquisition

Military system designers who want to save space and lower costs with data acquisition SBCs usually have to compromise. Either the processor's performance is lower than the application needs or the data acquisition functions are less capable. Fortunately, vendors



such as Diamond Systems are coming to the fore with workable alternatives. On a single board, the Poseidon EPIC form-factor SBC combines the VIA Eden ULV or VIA C7 processor running at speeds of up to 2 GHz with Diamond Systems' patented, automatically autocalibrating A/D circuitry. The connector board is removable, providing pin headers for a more rugged interface.

The Poseidon includes 256 Kbytes of on-chip cache, a 400 MHz front-side bus and up to 512 Mbytes of onboard soldered 533 MHz DDR2 RAM. The VIA CX700 integrated digital media chipset integrates the VIA UniChrome Pro 2D/3D graphics controller with integral MPEG-2 hardware acceleration, CRT and LVDS flat panel support, and dual independent display capability. The Poseidon SBC also provides four USB 2.0 ports, two RS-232 ports, two RS-232/422/485 ports, IDE and SATA hard drive interfaces, and an Intel 82541 Gigabit Ethernet controller. Typical power consumption is under 10W.

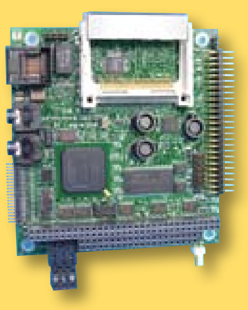
The board's data acquisition circuit incorporates the Diamond MM-32X-AT board, including 32 16-bit analog inputs with a 250 KHz sampling rate, four 12-bit analog outputs, 24 programmable digital I/O lines and two counters/timers. With the 1 GHz VIA Eden ULV processor, Poseidon operates fanless across an extended operating temperature range of -40° to +85°C. With the 2.0 GHz VIA C7 processor, it operates with a fan from -20° to +70°C. Prices start at under $700 in quantities of less than 10. Volume discounts are available.

Diamond Systems
Mountain View, CA.
(650) 810-2500.
[www.diamondsystems.com].

Low-Power Board Dynamically Changes Speed

Mobile military systems encounter constant change in the field. In those situations, electronics that dynamically alter processor speed in response to changing performance or power needs are a big plus. With that in mind, Micro/sys has based the design of its SBC1670 on the Intel PXA270 processor, which dynamically changes its speed in response to changing conditions. The SBC1670 combines an 800 x 600 color flat panel display interface with the low-power Intel PXA270 processor in a PC/104 footprint. The CPU's multimedia capabilities include support for audio output and debounced keypad input.

The PXA270 runs at speeds of up to 524 MHz. On-chip cache, a watchdog timer, an SDRAM controller, a CompactFlash interface and a USB host controller are integrated on the same silicon. The SBC1670 features 128 Mbytes of SDRAM, a 64 Mbyte resident flash array, five serial ports, four with RS-232 and one with RS-485, plus a 10/100BASE-T Ethernet controller. For expansion, a CompactFlash socket supports storage devices and I/O devices, such as Wi-Fi cards. Additionally, the SBC1670 has a 16-bit PC/104 bus interface, providing access to off-the-shelf boards such as modems, analog I/O or digital I/O. In its stackthrough version, the SBC1670 is ideal for plugging into a custom OEM I/O card.



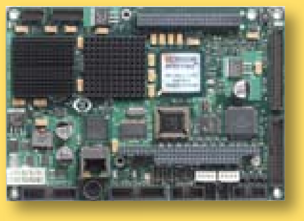
The SBC1670 can boot Linux, Windows CE and VxWorks from its onboard flash. A free development kit includes cables, sample software and full documentation. Pricing for the basic SBC1670 starts at $495 in single quantity. An extended temperature version operates from -40° to +85°C and is priced at $675.

Micro/sys
Montrose, CA.
(818) 244-4600.
[www.embeddedsys.com].

Rugged SBC Is Conduction-Cooled

In many defense and aerospace platforms, size, weight and power (SWP) are critical design considerations. Developed for applications that need all three, Octagon Systems offers the EPIC form-factor XE-900 SBC, designed to operate in harsh, demanding environments.

The XE-900 incorporates the 32-bit, low-power VIA Eden ESP CPU family. Three versions are available: the 400 MHz and 733 MHz versions operate at -40° to +85°C and the 1 GHz version operates at -40° to +75°C.



Memory includes 512 Kbytes of surface mount flash for BIOS, a SO-DIMM socket for up to 512 Mbytes of SDRAM and 1024 bytes of user-available serial EEPROM. ATA-4 hard drive and CompactFlash interfaces support up to three drives: CD-ROM, hard drive, EIDE flash drives and other EIDE devices. The board includes CRT and flat panel video, six RS-232/422/485 serial ports, two USB ports, 10/100 Base-T Ethernet, PC/104 and PC/104-Plus expansion and 24 lines of bit-programmable, digital I/O with 16 mA sink/source capability. It features ACPI 2.0 and PCI power management. The conduction-cooling system eliminates the need for a fan even at 1 GHz.

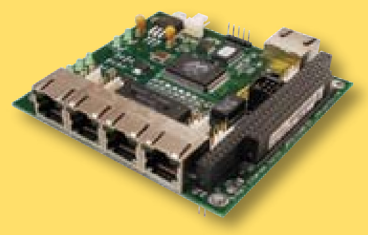
Companion XE-900 OS Embedder kits are available for Linux 2.6 and WindowsXP. These kits combine hardware and software for instant-on operation. The single piece price is $795 for the 1 GHz version, $745 for the 733 MHz version and $695 for the 400 MHz version. Volume discounts are available for all three.

Octagon Systems
Westminster, CO.
(303) 430-1500.
[www.octagonsystems.com].

VLAN-Enabled Switch Meets MIL-STD-810F

The military has its own unique needs when it comes to networking. Two of these that rank especially high are reliability and communications that are certifiably secure. To meet these needs, Parvus offers its PRV-1059, a VLAN-enabled five-port PC/104 Ethernet switch that has been designed and tested to MIL-STD-810F. This rugged network switch features very low power consumption at 1.5W and highly reliable extended-temperature operation up to +85°C.

Supporting auto-MDI-MDIX network installation, the board is designed for simple plug-and-play operation, enabling up to five embedded computing devices to be networked together using 10BaseT or 100BaseTX LAN connections. It also supports field-programmable, port-based VLAN functionality, enabling any combination of ports to be connected together in subnets for



use in a small secure or non-secure network. Settings are stored in local onboard memory. The board's five transceiver ports are fully compliant with IEEE 802.3 and IEEE 802.3u and any port can serve as an uplink.

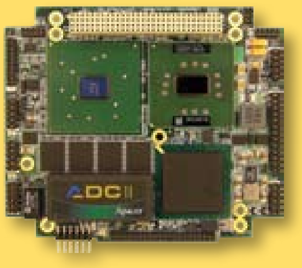
The card integrates fully independent media access controllers, an embedded frame buffer memory and a high-speed address lookup engine, along with support for auto-crossover, auto-polarity, auto-negotiation and bridge loop prevention. All versions include mounting holes to facilitate simple installation, as well as support for local or remote monitoring of LED activity for data RX/TX and connectivity. Pricing for the PRV-1059 is $199 for base models and $249 for models with VLAN support. Non-RoHS and RoHS-compliant versions are available.

Parvus
Salt Lake City, UT.
(801) 483-1533.
[www.parvus.com].

CPU Module, Controllers Feature PC/104-Plus, PCI-104

Fitting a high-performance embedded computer into the limited space available in many military applications is now easier, thanks to small footprint form-factors such as PC/104 SBCs. Even better are small SBCs that have been ruggedized. Serving just such needs are RTD's high-performance PC/104-Plus and PCI-104 cpuModules and controllers. The boards are available with either Intel 1.4 GHz Pentium M or 1.0 GHz Celeron M processors.

Both CPUs support four PCI bus masters and feature BIOS-selectable thermal throttling, ACPI (Advanced Configuration and Power



Interface) and APIC (Advanced Programmable Interrupt Controller). Nonvolatile BIOS configuration allows storage of CMOS settings with no battery required. Each SBC features 512 Mbytes of surface-mount BGA ECC DDR SDRAM and one ATA/IDE disk chip socket for an onboard IDE flash drive of up to 4 Gbytes that is natively supported by all major GPOSs and RTOSs.

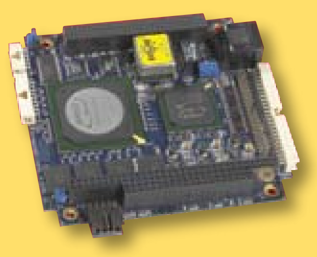
RTD's latest I/O technologies include two or four USB 2.0 ports and the RTD exclusive multiPort with BIOS selectable aDIO Advanced Digital I/O consisting of 18 or 36 digital I/O bits, ECP/ EPP parallel port or floppy drive. Standard PC I/O includes SVGA, LVDS flat panel, 10/100 Mbit Ethernet, AC'97 audio, BIOS-selectable RS-232/422/485, keyboard, PS/2 mouse and EIDE controller with UltraDMA-100. Wake events include aDIO interrupt, Ethernet, power button, serial port activity, USB and onboard real-time clock. The Pentium M also features advanced power management including Enhanced Intel SpeedStep Technology. Pricing is $2,795 for the Pentium M 1.4 GHz version and $1,995 for the Celeron M 1.0 GHz version.

RTD Embedded Technologies
State College, PA.
(814) 234-8087.
[www.rtd.com].

Rugged, Low-Power SBC Targets Harsh Environments

Most military systems require highly reliable operation under extreme environmental conditions. The ability to fit into small spaces and extremely low power consumption are also high on the demand list. Fortunately, vendors such as VersaLogic continue to roll out new products aimed at those needs. The company's PC/104-Plus Puma board not only delivers a highly reliable design and low power draw at under 5W typical total power consumption, but also includes a Windows-compatible suspend-to-RAM power management system that reduces power draw to less than 900 mW during standby.

Based on the AMD GX 500 processor, the RoHS-compliant Puma is fanless with no moving parts, and is offered in both standard temperature (0° to +60°C) and extended temperature (-40° to +85°C) versions. Standard onboard features include 256 Mbytes of soldered SDRAM, three COM ports, four USB 2.0 ports, Ethernet, IDE, LPT, audio I/O and keyboard/mouse/floppy support via USB ports. The board also includes integrated SVGA video with LVDS flat-panel support. The PC/104-Plus interface supports both ISA and PCI add-on modules. Standard pass-through connectors allow the board to be used either above or below other PC/104 modules. By plugging it into a proprietary baseboard that includes user



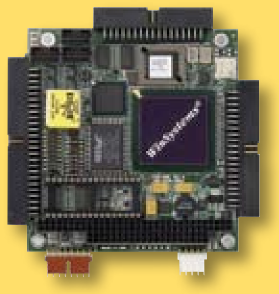
I/O circuitry, it may also be used as a CPU module for a larger system.

The Puma's customizable, OEM-enhanced BIOS is field-upgradeable. Windows CE/XP/XPe, Linux, VxWorks and QNX are supported. Pricing is approximately $550 in low OEM quantities.

VersaLogic
Eugene, OR.
(541) 485-8575.
[www.versalogic.com].

Compact Board Needs Only +5V, 900 mA

Although no two military applications are alike, military designers creating subsystems for small, lightweight systems need processing muscle in a low-power, minimum-sized package. With that in mind, WinSystems offers its PCM-SC520-G, a PC/104-compatible, RoHS-compliant SBC that requires only +5V and, with 32 Mbytes of SDRAM onboard, draws just 900 mA typical. The board includes soldered down DRAM and requires no fan for operation in rugged environments.



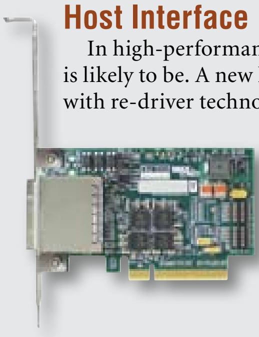
The PCM-SC520-G is based on AMD's highly integrated, 32-bit, low-voltage, 133 MHz AM5x86 SC520 CPU, with a complete set of integrated PC/AT-compatible peripherals. The CPU core includes a floating-point unit as well as enhancements to the PCI controller and synchronous DRAM controller to optimize it for applications requiring high throughput and low latency. The PCM-SC520 runs x86-compatible software over a temperature range of -40° to +85°C. It supports 32, 64, 128, or 256 Mbytes of SDRAM that is field-upgradeable from a standard SODIMM socket. For high shock and vibration environments, the board can be ordered with 32 Mbytes of soldered-down SDRAM. Up to 8 Gbytes of flash memory can be installed as a CompactFlash card or an M-Systems DiskOnChip flash device.

Included are four serial COM ports and a 10/100 Ethernet port. The onboard Intel 82559ER integrated Ethernet controller has a 32-bit PCI interface that supports 10/100 Mbit/s data transfers in full- and half-duplex modes. Four 16C550-compatible UARTs support RS-232 serial asynchronous data communications up to 115.2 Kbits/s. RS-422/485 levels are supported on COM 1 and 2. Other onboard peripherals include a floppy disk controller, IDE hard disk interface, keyboard controller, line printer interface, mouse port, battery-backed real-time clock, precision power-fail reset circuit and programmable watchdog timer. The board supports Windows CE, Linux and other x86-compatible operating systems, including DOS. List price is $429.

WinSystems
Arlington, TX.
(817) 274-7553.
[www.winsystems.com].

Products

Host Interface Board Extends PCIe Bus at x8 Speeds

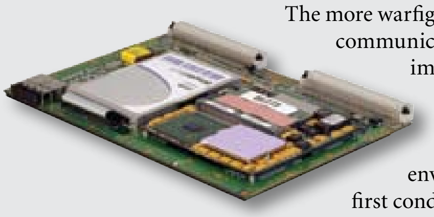


In high-performance military applications based on PCI Express, the more downstream PCIe boards there are, the slower communications is likely to be. A new host interface board (HIB) from One Stop Systems installs in a PCIe x8 or x16 slot and operates at 20 Gbits/s. It is designed with re-driver technology, boosting the high-speed signal over a PCIe cable to a downstream board. The downstream system acts as if it resides in the host system. The HIB2 extends the host bus over a high-speed PCI SIG-specified data cable. This connects to the upstream port of the company's chassis- or rackmounted 1U PCIe switch, further increasing the extendibility of the single host to over 100 add-in boards.

The HIB2 also supports a downstream link in non-transparent mode to a second host system. This configuration allows host-to-host communication with up to two 20 Gbit/s links for a total bandwidth of 40 Gbits/s. The HIB2 is available in host mode and target mode, using a target backplane and external PCIe card. It lists for $433.

One Stop Systems, Escondido, CA. (760) 745-9883. [www.onestopsystems.com].

VME NAS System Takes Aim at Severe Environments



The more warfighters depend on communications networks, the more important it becomes to secure those networks and their data, as well as protect equipment from harsh environments. The industry's first conduction-cooled Network Attached Storage (NAS) system, the INDEX VCNAS from General Micro Systems, supports up to 200 Gbytes of rotating media or a flash drive of up to 128 Gbytes in a single slot (4HP) VME form-factor. The unit's operating temperature range is -40° to +85°C and it complies with MIL-STD-810-F. Embedded error correction and detection algorithms are employed for the solid state drive that yield a data error rate of less than 1 bit in 10^{14} bits read. Rapid Purge, MilPurge and Intelligent Destructive Purge modes provide advanced content protection.

The VCNAS is based on General Micro Systems' STRONGHOLD VC266 VME 6U SBC, powered by a 1.8 GHz Intel Pentium M processor with up to 2 Gbytes of memory for protocol and packet work, and up to 266 MHz DDR SDRAM and ECC. Dual Gigabit Ethernet ports may be configured as fiber on the front panel, or via rear I/O or VITA 31.1. Dual video for RGB or LCD monitors is supplied. The VCNAS supports Windows XP/2000, VxWorks-Tornado II, Solaris x86, QNX and Linux. Pricing starts at $4,200 in 100 units.

General Micro Systems, Rancho Cucamonga, CA. (800) 307-4863. [www.gms4sbc.com].

6U VME SBC with Intel Core Duo Targets Mil Apps

Military VME system integrators looking to take advantage of Intel's dual-core performance and low power consumption now have a ruggedized platform designed for harsh environments. The SVME/DMV-1901 6U VME SBC from Curtiss-Wright Controls Embedded Computing features the Intel Core Duo processor running at 1.67 and 2.0 GHz. A single-core Intel Core Solo is also available. The board comes with 2 Mbytes of L2 Advanced Transfer Cache, up to 4 Gigabytes of ECC DDR2 SDRAM, up to 4 Gigabytes of USB user flash, Intel's E7520 Memory Controller Hub, Intel's 6300ESB I/O Controller Hub and onboard ATI Radeon X300 Graphics with 4-lane PCI Express.

In addition to two PMC/XMC mezzanine expansion sites, the SVME/DMV-1901's I/O includes two Gigabit Ethernet ports, two video graphics ports, three USB 2.0 ports, six COM ports, two SATA ports, eight GPIO lines, AC'97 audio, two PS/2 ports and two SCSI ports. Air-cooled front panel I/O includes onboard video graphics and SCSI interfaces. WindowsXPe, Solaris10 and Linux are supported. The SVME/DMV-1901 L0, L50 and L100 air-cooled and L100 and L200 conduction-cooled configurations are available. Volume pricing for the air-cooled SVME-1901 starts at under $4,700.

Curtiss-Wright Controls Embedded Computing, Leesburg, VA. (703) 779-7800. [www.cwcembedded.com].

Analyzer Supports 5 Gbits/s Per Lane PCIe

Military engineers developing systems at faster bus speeds face a lot of challenges. One thing that will help is a PCI Express protocol analyzer that captures and analyzes second-generation PCI Express bus traffic at data rates of up to 5 Gbits/s per lane. The PE Tracer Gen2 Summit x16 from LeCroy locates errors faster and records and displays all traffic, even at high lane widths and data rates. The analyzer's real-time monitoring tools analyze response and latency of transactions, data throughput and link utilization. It works with the company's PE Tracer software, which features real-time statistics, protocol traffic summaries, detailed error reports, scripting and creation of user-defined test reports. Ethernet and USB ports are provided for connection and configuration flexibility.

The PE Tracer Gen2 Summit x16 supports spread-spectrum clocked traffic, lane swizzling for flexibility in board configurations, auto-link sensing for links of varying width and support for multi-link operations where PCI Express ports are bifurcated into narrower links. Raw Mode Recording records bytes as they come across the link, allowing debugging of PHY layer problems and combining the features of a logic analyzer format with a decoded protocol analyzer display.

LeCroy, Chestnut Ridge, NY. (845) 425-2000. [www.lecroy.com].

PXIe Data Acquisition Modules Target High Channel Counts

PXI boards have become entrenched in the military as solutions for testing complex system designs. Now, two data acquisition modules from National Instruments designed for high-channel-count applications are the first in the industry for PXI Express, according to the company. The NI PXIe-6259 and PXIe-6251 M Series modules deliver fast analog and digital I/O with a dedicated per-slot bandwidth of up to 250 Mbytes/s. They feature up to 32 analog channels with 16-bit, 1.25 Msamples/s sampling speed, up to four analog output channels with 16-bit, 2.8 Msamples/s update rates and 10 MHz digital I/O on up to 32 lines.

As with other NI M Series DAQ devices, the new PXI Express modules feature the NI-STC 2 system controller, the NI-PGIA 2 amplifier and NI-MCal calibration technology for increased performance, accuracy and I/O. They work with all existing PXI modules and software. Existing code written for the NI LabVIEW graphical development platform, NI LabWindows/CVI ANSI C development environment and NI Measurement Studio for Microsoft Visual Studio can be used with them. The NI PXIe-6259 and NI PXIe-6251 M Series modules are priced from $1,149.

National Instruments, Austin, TX. (512) 683-0100. [www.ni.com].

Digital RCVR Board Eliminates FPGA Development Tasks

Developers of real-time DSP and software radio systems often want to avoid the lengthy, complex programming that can accompany the use of FPGAs. With the GateFlow Model 6821-422 high-speed A/D digital down-converter (DDC) board from Pentek, now they can. The board includes a factory-installed wideband digital down-converter FPGA IP core operating at frequencies of up to 296 MHz. It is a highly optimized, dual-channel version of Pentek's GateFlow IP Core 422 tailored to the board's various resources. The result is a preconfigured, fully tested digital software radio subsystem that accepts a front-panel analog RF input and delivers real or complex digital output samples translated to baseband from any frequency slice of the input signal. The board has a 12-bit sample rate at 215 MHz and four sets of user-programmable FIR coefficients for custom filtering.

The Model 6821-422 is supported by Pentek's C-callable ReadyFlow Board Support Libraries. ReadyFlow provides development tools for quick startup through application completion, allows programming at high, intermediate and low levels to meet various needs, and includes complete source code for all functions. Ruggedized and conduction-cooled versions of the board are available. Pricing starts at $17,495.

Pentek, Upper Saddle River, NJ. (201) 818-5900. [www.pentek.com].

Mini-ITX Motherboard Features Intel Core Duo

New military system designs may need faster processing speeds but be constrained by power and heat limitations. Dual-core processors can deliver up to twice the performance for far less than twice the heat. The RoHS-compliant G5C100-N-G Mini-ETX motherboard from ITOX Applied Computing is equipped with the Intel Core Duo processor and supports the Core Solo, as well as the Celeron M and Celeron M ULV CPUs. It utilizes the 945GM Express chipset paired with an ICH7M I/O controller hub, as well as up to 4 Gbytes of 533 MHz or 667 MHz DDR2 dual-channel memory, dual onboard PCI Express Gigabit Ethernet controllers and Intel GMA 950 graphics. A single mPGA 479 socket provides support for specified Intel processors with 667 MHz, 533 MHz and 400 MHz system bus speed.

For connectivity, the board has two Gigabit LAN ports, four serial COM ports, eight USB 2.0 ports, two PS/2 ports, a VGA port (2048x1536), 1-LVDS DFP Interface (1600x1200), Onboard 5.1 channel Audio with S/PDIF out, two SATA interfaces, an Ultra ATA 100 interface, a CompactFlash Type II socket and an FDD interface. List price is $468.

ITOX Applied Computing, East Brunswick, NJ. (888) 200-4869. [www.itox.com].

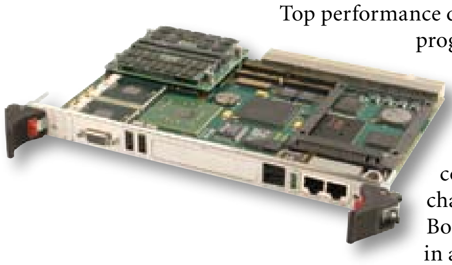
Storage Module Brings Fibre Channel SAN to Rugged Environments

Using commercial Fibre Channel disks for high-speed, streaming data recording applications in harsh environments such as aircraft would allow the power, flexibility and ease of use of the Fibre Channel Storage Area Network (SAN) to be fully exploited. Now this is possible, with VMetro's SANbric storage system. The rugged, removable storage device provides 1.8 terabytes of storage capacity in a JBOD (Just a Bunch of Disks) configuration in only 4U of shelf space.

The SANbric connects to the Fibre Channel SAN via dual 2 Gbit/s Fibre Channel interfaces. Each interface connects to a loop on the SANbric's backplane, which is split for the dual-loop operation necessary for 400 Mbyte/s sustained throughput (300 Mbytes/s on the inner tracks). The backplane connects to six 3.5-in. Fibre Channel disk drives. Utilizing a shock isolation frame, the SANbric is designed to tolerate the shock, vibration, altitude and temperatures of extreme environments such as image processing and sensor processing applications in UAVs and other aircraft. Price is $49,900.

VMetro, Houston, TX. (281) 584-0728. [www.vmetro.com].

Two Dual-Core ULV Xeons Fit on Single-Slot 6U SBC



Top performance density and ease of programming for symmetric multiprocessing are two things really needed by military engineers developing computationally challenging applications. Both are now available in a family of SBCs from Mercury Computer Systems that incorporates one or two 1.66 GHz Dual-Core Intel Xeon ULV processors in a 6U single-slot module. The board's density is made possible by the ULV processor, with a thermal design power of only 15W. First in the family of CompactPCI or VME boards is the cPCI Momentum Series CX6-200. On each board, both dual-core processors are connected in a symmetric multiprocessing (SMP) configuration, so each processor core has easy access to 8 Gbytes of shared memory.

PCI Express technology minimizes internal data-flow bottlenecks and maximizes external I/O throughput for onboard interconnects. I/O includes quad Gigabit Ethernet, RS-232 serial I/O, high-speed serial ATA-150, USB 2.0 and SVGA, with most available at the front panel for easy connectivity. A single-wide PMC/XMC expansion site supports both front and rear I/O. Pricing for the Momentum Series CX6-200 starts at $6,295 each. Discounts are available for higher volumes.

Mercury Computer Systems, Chelmsford, MA. (978) 256-1300. [www.mc.com].

Single-Slot Dual Removable VME Hard Disk Rolls

As military systems continue to push for more and more embedded computing, the need for rugged storage is accelerating. Feeding such needs, Phoenix International has added a Dual Removable Hot-Swap Disk Drives option to its line of Rugged Mass Storage VME plug-in modules. The new VF1-250-SC-RHD model allows portability in transporting a data storage device (by itself) for secure or archival storage off-line or for transferring data files to operating storage arrays, servers or host platforms. The dual device configuration is ideal for host-based RAID 1 (data mirroring) applications as it is designed to allow the user to hot-swap either or both hard disk drives from a standard single-slot (4HP) 6U plug-in VME module.

Other features of the VF1-250-SC-RHD include transparency to any operating system, Ultra-320 LVD SCSI I/O, 10,000 RPM spindle speed and an average Seek Read/Write time of 4.1 and 4.5 msec respectively. SCSI connect is done via front panel and/or back plane P2 connectors. The unit supports automatic internal bus termination and sports front panel device ID select and activity indicator. The device features rugged steel construction with internal heat sink. MTBF is rated at 1,400,000 hours.

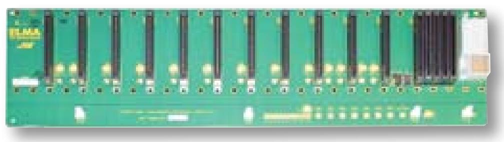
Phoenix International, Orange, CA. (800) 203-4800. [www.phenxint.com].

3U PXI Power Analyzer Module Targets RF Communications

Compact test solutions based on PXI are being deployed increasingly in wireless defense communications. One example is the GX2002 RF Power Analyzer, developed jointly by Geotest-Marvin Test Systems and ZTEC Instruments. The 3U PXI card provides the ability to perform CW and pulse power measurements, frequency measurements and pulse repetition period measurements on RF signals from 100 MHz to 3 GHz.

The GX2002 includes a full-featured user interface and drivers for ATEasy and other popular software development environments. The module includes an onboard DSP engine that can acquire, process and store frequency, pulse width, pulse repetition interval peak power and time-tag for each RF input pulse in less than 200 microseconds. Pricing starts at $2,995.

Geotest-Marvin Test Systems, Irvine, CA. (949) 263-2222. [www.geotestinc.com].



14-Slot MicroTCA Backplane Provides More Connections

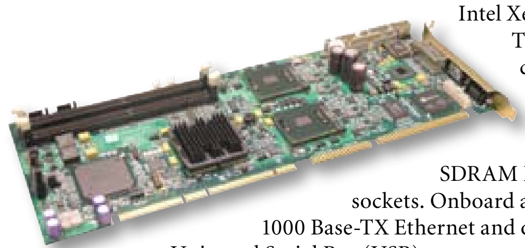
Interest in MicroTCA continues to build among military system designers, since the architecture lets AMC modules be plugged directly into a backplane to create small, low-cost but powerful systems. A 14-slot single-star MicroTCA backplane from Elma Bustronic allows single or redundant virtual carriers to provide power management, platform management and fabric connections to greater numbers of modules than a single physical carrier card could support in a classic ATCA application.

The unit has 12 AMC slots, a power module slot and a MicroTCA controller hub (MCH) slot in the single-width, full-size format. It features a 16-layer controlled-impedance stripline design. Pricing for the 14-slot MicroTCA backplane is under $500 depending on volume and configuration.

Elma Bustronic. Fremont, CA. (510) 490-7388. [www.elmabustronic.com].

Passive Backplane SBC Sports Dual Core Xeons

There's no side stepping the industry trend toward dual-core and multicore processors. Because pipelining and superscalar tricks can only go so far, all the major microprocessors have dual-core offerings dominating their future roadmaps. Riding that trend, Diversified Technology (DTI) announced the release of the LBC9426 single board computer for communications, government and commercial markets. The LBC9426 is based on the Intel E7520 chipset and utilizes 1 or 2 dual-core Intel Xeon Low Voltage Processors.



The LBC9426 industrial single board computer features one or two 65 nm Dual Core Xeon processors with 2 Mbyte L2 cache Micro-FCPGA processors and up to 8 Gbytes dual channel, DDR2 SDRAM DIMMs, with full ECC support, on two sockets. Onboard are two channels of 10 Base-T, 100 Base-TX, 1000 Base-TX Ethernet and dual Serial ATA channels, as well as four Universal Serial Bus (USB) ports, two serial ports, a parallel port, floppy interface and a PCI VGA and flat-panel controller with 8 Mbytes of memory. The LBC9426 uses the Intel E7520 chipset providing a 667 MHz system bus as well as one x4 PCI Express Link. The single x4 PCI Express link provides access to a dual-port Gigabit Ethernet controller allowing multiple high-speed offboard data transfers.

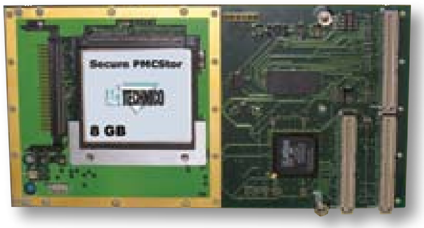
Diversified Technology, Ridgeland, MS. (601) 856-4121. [www.diversifiedtechnology.com].

Data Acq System Accommodates Multiple cPCI Digitizers

It used to require a large rackmounted data acqusition apparatus to do high throughput measurements and analysis for military systems. Now that same functionality is possible in a compact system that can be run from a PC. Along such lines, Acqiris now offers the MAQlink3000, 5000 and 8000 systems, which can accommodate multiple 8-, 10- and 12-bit CompactPCI digitizers. Each includes a high-speed interface for desktop PCs or laptops so acquired data can be processed by the highest-speed processors. In addition to the PC interface, the MAQlink systems can accommodate up to 28 high-speed acquisition channels. These channels are all controlled through Acqiris' unique AcqirisMAQS multichannel acquisition software installed on the interfaced PC.

With AcqirisMAQS, a client-server software suite, vital information can be seen with a multiple waveform display on the PC monitor. Data is more accessible with an oscilloscope-like graphical user interface (GUI). MAQlink's modularity enables users to select only the hardware components needed for a specific application and expand to a larger system as needs grow. This helps reduce instrument obsolescence and increases return on investment. Pricing for a MAQlink system starts at $5,790.

Acqiris USA, Monroe, NY. (877) 227-4747. [www.acqiris.com].



PMC Storage Solution Provides Secure Erase

Whether it's ground mobile, shipboard or airborne systems, there's no room for error when it comes to protecting classified or sensitive data. ACT/Technico is helping the situation with a new secure storage solution that provides an effective means to perform secure erasure or write-protection of sensitive data on a PMC form-factor. The Secure PMCStor provides a unique hardware-based implementation of two methods of data protection: Secure-Erase, with two levels of data purging; and Write-Protect, preventing data from being overwritten or modified. It couples a PCI/ATA core with secure-erase and write-protect logic implemented via an FPGA.

The Secure PMCStor features a hardware-initiated Secure-Erase with two erasure levels—destructive or non-destructive; a Write-Protect function enabled via an external signal or switch; and the provision for onboard BIOS supporting system boot directly from the storage device. The new storage solution is available with one or both data security features, and is suitable for extended temperature in air- and conduction-cooled environments. The air-cooled version ships with a front panel button or switch to initiate the secure features. The Secure PMCStor is fully tested prior to shipment. Storage capacities range from 2 Gbytes to 16 Gbytes.

ACT/Technico, Ivyland, PA. (215) 957-9071. [www.acttechnico.com].

DC/DC Converter Series Is Designed for Battle

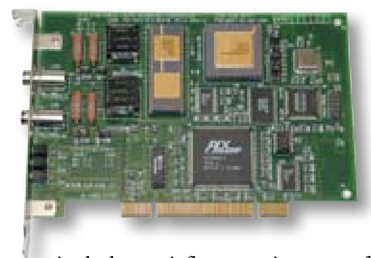
Battlefield military applications put a lot of stress on DC/DC converters. Ensuring smooth operation in extreme shock, vibration and weather conditions is no easy task. XP Power has met those challenges with its new MTC, a series of 4W to 35W DC/DC converters designed exclusively for defense and avionics applications. Available in 5, 15 and 35W ratings, the converter meets the MIL-STD 810F specification for temperature, shock, vibration, bump, altitude, salt fog and other key parameters. Input immunity with the complementary filter module, designated MTF, meets MIL-STD 1275A/B and MIL-STD 704A. EMI performance meets MIL-STD 461E with the filter installed.

Single output versions are available with output voltages of 3.3V, 5V, 12V, 15V or 28V. The MTC is fully featured to minimize external circuitry. It includes an inhibit line, the ability to synchronize with an external frequency source, output voltage programmable by resistor or external voltage, thermal warning "battle mode" signal on the 35W units, over-voltage protection and over-current protection. Both the MTC and MTF are available now. The MTC is priced from $120 each for the 4W unit to $260 each for the 35W version. MTFs are $170 each. All prices are based on 100+ quantities.

XP Power, Littleton, MA. (978) 287-7260. [www.xppower.com].

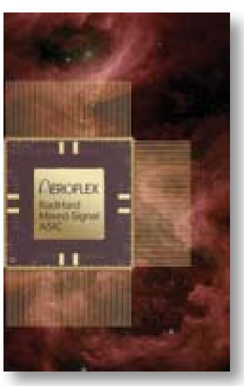
PCI Card Supports All 1553 Bus Modes

Despite its age, the MIL-STD-1553 data bus standard remains a popular solution as a deterministic interface control technology. Targeting 1553 system developers, Alphi Technology has announced the PCI-1553-PLX-x. It implements a complete single-channel, dual-redundant MIL STD-1553 bus terminal on a half-size PCI Card. Operating with 5V or 3.3V VIO signaling, the board supports Full Bus Controller, Remote Terminal and Bus Monitor modes. Support is provided for both direct coupled (short stub) and transformer coupled (long stub) configurations. Features include a bus master interface, flexible processor to memory interface, external 64 kword SRAM, external clock inputs, front panel I/O connectors and onboard transceivers and transformers.



The PLX 9080 PCI-x's standard operating temperature is 0° to 70°C, with support for -20° to 85°C. Non-operating temp range is -40° to 85°C. Other environment specs include an airflow requirement of .5 CFM, humidity from 5 to 90% (non-condensing), altitude range from 0 to 10,000 ft, vibration capabilities at 0.5G RMS 20-2000 Hz random and shock of 20G, 11 ms, one-half sine. Software libraries and drivers are available.

Alphi Technology, Tempe, AZ. (480) 838-2428. [www.alphitech.com].



Mixed-Signal ASICs Boast Rad-Hardening

For space applications, there's no sending a repairman to fix a faulty chip. That's why radiation-hardened components are vital for spaceborne systems. Serving that need, Aeroflex has announced the addition of RadHard Mixed-Signal ASICs to their RadHard product line. Aeroflex's RadHard Mixed-Signal ASICs combine high-performance analog with digital logic and will be offered in 0.6 um (5V) and 0.35 um (3.3V to 10.0V). Specializing in precision data conversion products, Aeroflex's analog IP includes ADCs—up to 21-bits resolution—and DACs, along with embedded voltage references, op amps, sample-and-hold and analog muxes.

The RadHard Mixed-Signal ASICs will meet the same radiation-hardened specifications as Aeroflex's Digital ASICs—100 krad (Si) to over 1 Megarad (Si) total ionizing dose," said David Kerwin, director, Mixed-Signal ASICs. The company is currently designing multiple RadHard mixed-signal ASICs in its commercial RadHard 0.35um Triple-Well CMOS process for customers, with first deliveries in 1Q07. Future plans include a RadHard 0.18um Triple-Well CMOS technology and RadHard standard data converter products for space applications.

Aeroflex, Colorado Springs, CO. (719) 594-8035. [www.aeroflex.com].

Batteries Deliver 3.6V at up to +125°C

Cost may be the key factor in consumer batteries, but for military users it's all about the energy density. The more energy the longer the life of the batteries, and that means longer missions. With that in mind, Tadiran, a supplier of lithium battery technology, has just introduced TLH Series lithium thionyl chloride cells, long life batteries that provide 3.6V of power in temperatures up to +125°C.

Available in all of Tadiran's standard cell sizes: 1/2AA, 2/3AA, AA, C, D and DD cylindrical cells as well as wafer cells, TLH Series cells offer twice the energy density of other leading chemistries as well as the widest operation temperature: -55° to +125°C. Maximum service life of the batteries is 20+ year. The small form-factor devices have a glass-to-metal hermetical seal, rather than the usual crimped elastomer gasket. Tadiran TLH Series lithium thionyl chloride batteries are also ISO-9001-certified and UL-recognized.

Tadiran, Port Washington, NY. (516) 621-4980. [www.tadiranbat.com].

Multiplexing Converter Unit Targets Tactical Nets

As the DoD transitions to fully Net-Centric operations, fast, reliable networking gear like multiplexing protocol converters are becoming critical building blocks. Ultra Electronics-DNE Technologies has announced a new, modular multiplexing protocol converter for use in tactical networks. The product, called the CV-MCU2, can be software-configured to perform CDI/NRZ/Fiber conversions or up to 4:1 multiplexing in a single 1-RU chassis. The CV-MCU2 allows the tactical user to configure a single unit as either a multiplexer or a modem, or any combination of the two, allowing the circuits to operate independently or be combined as needed without replacing hardware modules when a reallocation of circuits is required.

A universal copper/fiber/NRZ module used in the CV-MCU2 provides both an increase in port density and circuit flexibility to the tactical user, supporting up to five 20 Mbit/s protocol conversions per 1-RU chassis. In addition, these modules now provide interoperability with deployed Canoga Perkins 2270 Fiber Optic Modems, allowing the CV-MCU2 to be a viable space-saving alternative when installing new modems in tactical communications vans. All cards are hot-swappable and can be configured via a front-panel LCD interface, or through Serial DB-9 or Telnet RJ-45 ports.

Ultra Electronics-DNE Technologies, Wallingford, CT. 1-800-370-4485. [www.ultra-dne.com].

Linux Development Platform for XScale CPU

The Intel XScale processor architecture has become a popular choice for low-power, high-compute-density designs. Those characteristics fit nicely into the emerging demand for nanocomputing in next-gen military programs. Supporting that trend, Arcom has released a new entry-level embedded Linux Development Kit to support its ultra-low-power PXA255 Xscale-based single board computers. The 400 MHz VIPER and 200 MHz VIPER-Lite are small footprint SBCs powered by the PXA255 ARM-compatible RISC processor.

The entry-level VIPER / VIPER-Lite Development Kit for embedded Linux features a compact implementation of the GNU/Linux operating system based on the standard 2.6 Linux kernel release. This has been optimized for use on Arcom's PXA255 platforms and is pre-loaded and configured into the embedded Flash. The Development Kit is available with two board options, the fully populated 400 MHz VIPER PC/104 single board computer, or the 200 MHz VIPER-Lite. The Development Kit includes the VIPER-I/O interface board (offering a selection of opto-isolated I/O ports) and a converter module to drive a regular analog VGA display. Price for the VIPER-Lite for Linux kit starts at $495.

Arcom, Overland Park, KS. (913) 549-1000. [www.arcom.com].

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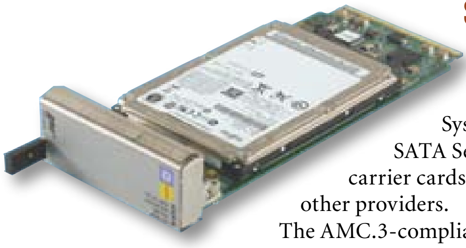
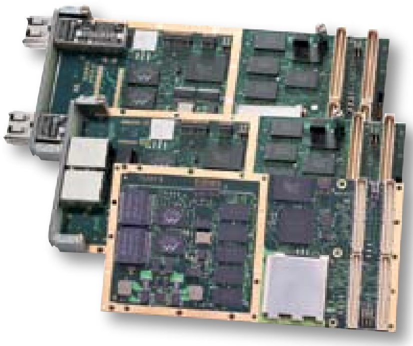


Serial ATA Hard Drive Module Climbs onto AMC

It's too soon to tell whether or not AMC and MicroTCA will make a big splash in military applications. But all indications are that they have what it takes to gain acceptance there, particularly in benign, non-harsh environment applications. With that in mind, GE Fanuc Embedded Systems has announced its new Telum 200-SATA AdvancedMC hard drive module. The Telum 200-SATA Serial ATA hard disk drive module is designed for use with AdvancedTCA single board computers and carrier cards from GE Fanuc Embedded Systems' extensive line of embedded products, and also with those from other providers.

The AMC.3-compliant Telum 200-SATA AdvancedMC module provides large capacity storage for AdvancedTCA and MicroTCA systems. The serial ATA (SATA I) hard disk drive offers capacities up to 100 Gbytes. An onboard multiplexer is provided for common options region ports two or three. The unit features Intelligent Platform Management Interface (IPMI) and hot-swap capability, and works in both standard and continuous operating mode. The AMC.3-compliant Telum 200-SATA AdvancedMC module is available in multiple configurations, including standard or continuous operation (extended duty cycle) hard drives.

GE Fanuc Embedded Systems, Albuquerque, NM. (505) 875-0600. [www.sbs.com].



Gbit Ethernet Controller Features Advanced TOE

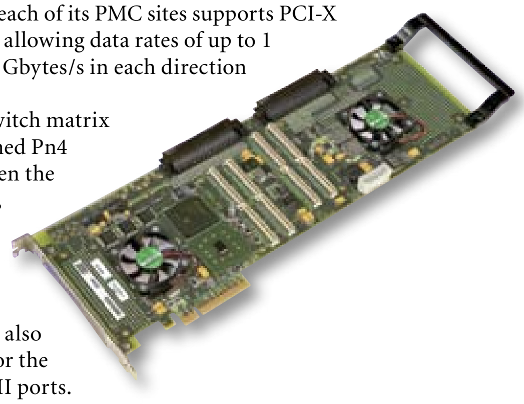
The military is entrenched in its growing affection for Ethernet. It offers both the ubiquity and longevity that are critical in the defense world. Feeding those needs, Data Device Corp. (DDC) has announced the production release of its next-generation ET-71000 GigExtreme Intelligent Gigabit Ethernet Network Access Controller (NAC). Featuring DDC's TCP/IP Offload Engine (TOE) technology, the extended-temperature NAC is currently being implemented in a USAF bomber upgrade program.

By offloading the entire TCP/IP stack, DDC's ET-71000 series' TOE reduces host utilization to less than 5%, compared to 50% or higher processor loading experienced with standard Gigabit Ethernet interfaces. A transparent host driver implemented using a standard TCP/IP socket interface, enables operation of the ET-71000 without modification to the network application. The cards are conduction-cooled, with front and rear panel network interface options, operate over a wide -40° to +85°C temperature range, and feature a dual-redundant architecture.

Data Device Corp. Bohemia, (631) 567-5600. [www.ddc-web.com].

PCIe Dual PMC Carrier Card Delivers 8 Lanes, FPDP

A new full-length PCI Express carrier card is reputedly the first to support eight lanes of PCIe I/O and dual FPDP connectors, giving military system designers higher data transfer rates than are possible with conventional parallel buses. The ICS-7003 from ICS, part of Radstone Embedded Computing, provides a platform for subsystem blades based on two PMCs. It includes a PCI Express to dual PCI-X bridge, and each of its PMC sites supports PCI-X (64-bit, 133 MHz), allowing data rates of up to 1 Gbyte/s, or up to 2 Gbytes/s in each direction simultaneously.



An intelligent switch matrix provides user-defined Pn4 connections between the two PMC modules, entirely avoiding the host processor and operating system. The switch also provides support for the board's two FPDP II ports. Installation into 8-lane or 16-lane PCIe systems requires no additional drivers. Pricing begins at $2,964.

Radstone Embedded Computing, Billerica, MA. (800) 368-2738. [www.radstone.com].

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Coming Next Month

Coming Next Month in November *COTS Journal*

- *Power Conversion.* Once relegated to an afterthought in the system design process, power supplies and power conversion electronics now rank as a make or break technical choice in embedded military computer systems. With more and more computing stuffed into smaller spaces, power has direct implications on the size, cooling and mobility of a system. Articles in this section examine technology trends affecting DC/DC converters, power supply module bricks and slot-card power supplies (VME, cPCI and others).
- *Stand-Alone Rugged Boxes.* A trend has been gathering momentum in the past couple years whereby traditional embedded board vendors are adding stand-alone rugged box-level systems to their military market offerings. These complete system boxes—which often support standard form-factor boards inside them—provide a complete, tested and enclosed computing solution that eliminates complex integration chores for customers. This section looks at this emerging product class and outlines the problems it solves.
- *JTRS HMS Design Considerations.* The DoD's Joint Tactical Radio System (JTRS) has traveled a rocky road, but it's off and running after a major rescoping of the program earlier this year. As part of the reorg, JTRS Cluster 5 radios were redesignated "Handheld/Manpack/Small Form Fit" (HMS) radios. Articles in this section focus on this portion of JTRS with an overview of the critical size, weight and power design considerations particular to this category of radios.
- *Fibre Channel Boards.* Fibre Channel boasts proven success in commercial markets along with a solid set of mature specifications and standards, with work on-going toward higher performance levels. Fibre Channel remains popular as a back-end link to storage in radar, SIGINT and other military systems. It's seen as a "here today" alternative like switched fabric storage links. This Tech Focus section updates readers on Fibre Channel boards in PMC and other form-factors, and provides a product album of representative boards.

COTS

Editorial

Jeff Child, Editor-in-Chief

RoHS Isn't Another Y2K

It's with wry amusement that we look back at the hype and anxiety during the run up to January 1, 2000. When embedded clock circuitry on chips had to deal with "00" in their 2-digit year registers, many seriously expected the world to stop working. The problem ended up being more isolated and less dire than expected. And the phrase "Y2K" faded from view.

In many ways, the general commercial electronics industry woke up on the morning of July 1 able to put the European Union's RoHS behind them just as easily as Y2K. The major semiconductor vendors have by and large already made their complete shift over to RoHS compliance. And for the biggest chip markets like consumer electronics, boards and even end-user devices are now always disposed of rather than repaired. No issues there of long-term reliability or of mixing leaded and lead-free components in the same system.

The situation is not so rosy in the defense market. Ironically, the defense industry, while one of the industries that's exempt from the Restriction of Hazardous Substances (RoHS) initiative, is much more affected by it than other industries. That doesn't mean makers of board-level products, for example, are off the hook, because in this age of COTS most companies craft board designs targeted for both military and non-military markets. Even companies purely in the military market can't escape RoHS's effects because these days it would be extremely costly and inefficient not to use the chips and components designed for the commercial market. The only alternative would be boards populated with completely customized silicon.

It's clear that military and aerospace markets face some unique requirements. Much higher reliability requirements, extremely long service lifetimes (decades) and extended temperature ranges top the list. Add to that the fact that the DoD is among the few segments that actually repairs embedded computer boards, rather than just disposing of them when a component goes bad. Meanwhile, lead-free components face solder issues and tin whisker failures that aren't acceptable. Strategies to deal with those issues are immature at this point, and it's likely to be years before they're solved. And I doubt the U.S. DoD or other countries will jump the gun before there are satisfactory, well-verified solutions in place.

In the year or so leading up to the July 1 RoHS deadline, the DoD and other major defense industry institutions, quite frankly, were slow to show leadership on how to deal with RoHS. That said, there were efforts underway by the Lead-Free Electronics in Aerospace Project Working Group (LEAP-WG) of the AIA. Formed in 2004, the group was tasked to develop and implement documents describing best practices and technical guidelines to enable the aerospace industry and the military to accommodate the global transition to lead-free electronics.

Three of those documents prepared by LEAP-WG were released in mid-July. The first one, GEIA-STD-0005-1, Performance Standard for Aerospace and High Performance Electronic Systems Containing Lead-Free Solder, gives broad direction to defense and aerospace suppliers and manufacturers on customer "care-abouts" in the form of objectives, and requires suppliers to document the processes they will use to satisfy the objectives. Examples of objectives are quality and reliability, configuration control, repair and rework.

The second document, GEIA-STD-0005-2, is dubbed Standard for Mitigating the Effects of Tin Whiskers in Aerospace and High Performance Electronic Systems. Although many aerospace and defense electronics manufacturers will continue to use tin-lead as an attachment alloy for printed wiring assemblies, there will be little alternative to using parts with lead-free alloy finishes, the most common of which is pure tin. Pure tin finishes promote the growth of "tin whiskers," which can cause serious reliability problems in aerospace and defense systems. While the technical details of tin whisker growth and control are not completely understood, their effects must be controlled in aerospace and defense products. This standard provides a framework to do so. It is structured according to levels of mitigation, which are selected by aerospace and defense electronics manufacturers and users, based on the level of control required for the given application.

The third document, GEIA-HB-0005-1, Program Management/Systems Engineering Guidelines for Managing the Transition to Lead-Free Electronics, provides guidance for program and systems engineering managers for managing the use of lead-free electronics. Programs may inadvertently introduce lead-free elements (including component finish, printed wiring board finish, or assembly solder) if careful coordination between buyer and supplier is not exercised. This handbook is designed to assist programs in ensuring the performance, reliability, airworthiness, safety and certifiability of products, in accordance with GEIA-STD-0005-1.

To be released at a later date, the LEAP-WG is also working on two other documents: Technical Guidelines for Using Lead-Free Solder in Aerospace and High Performance Electronic Systems Containing Lead-Free Solder and Finishes, and Technical Guidelines for Reliability Testing for Aerospace and High Performance Electronics Containing Lead-Free Solder. According to the GEIA, all these documents will be eventually submitted to the International Electrotechnical Commission (IEC) for use as international standards.

So the good news is that the DoD has begun to provide guidance on dealing with the RoHS beast, although more definitely needs to be done. The bad news is that, unlike life after Y2K, we have to get used to the fact that life after RoHS, particularly for the defense industry, is something we'll have to deal with long after the morning after.